SiGe CVD, fundamentals and device applications

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Aixtron Inc

ICPS, Flagstaff July 2004

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Á *OVERVIEW*

1. Introduction

2. SiGe Market Survey

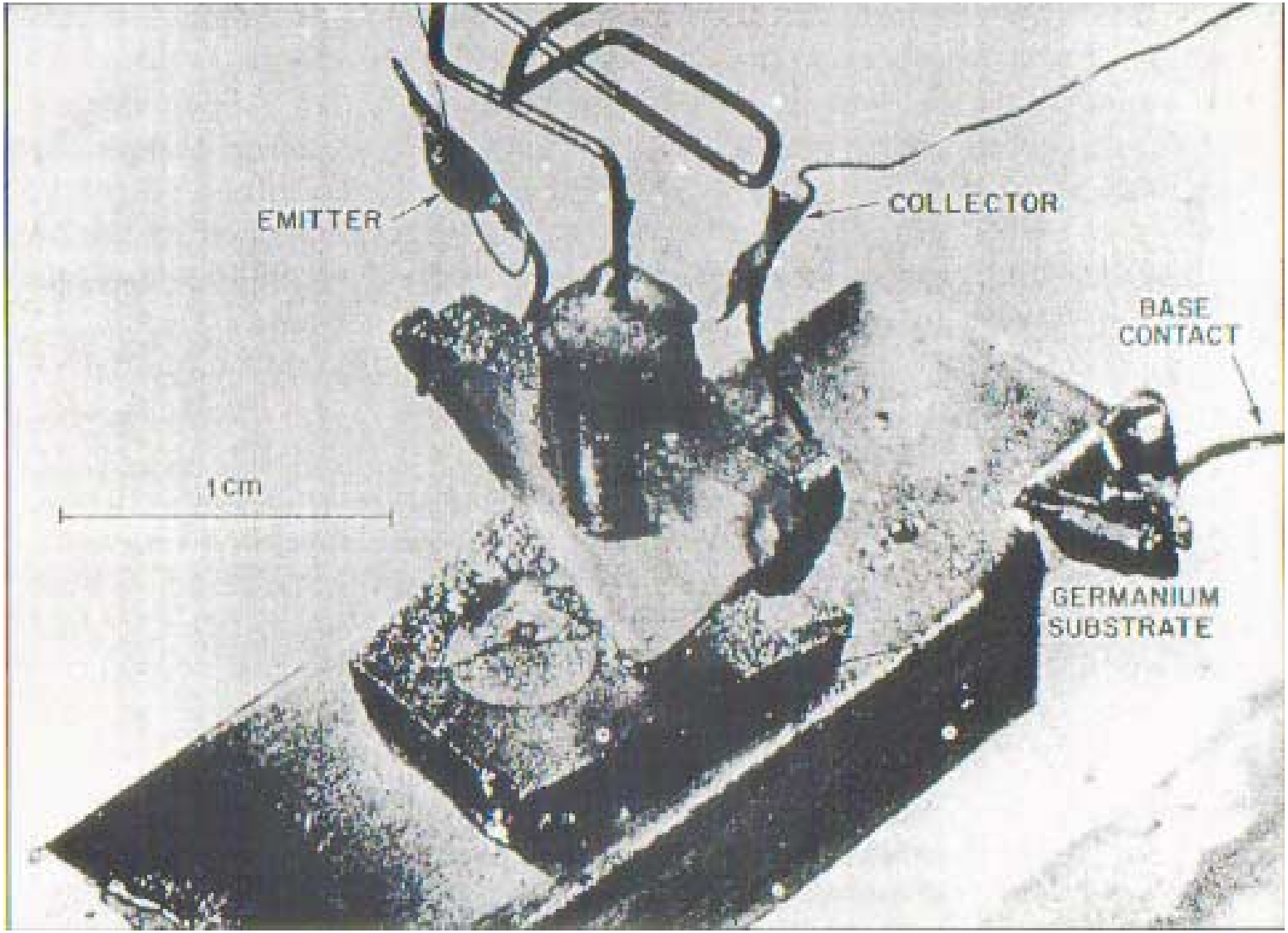
3. Fundamentals of SiGe CVD

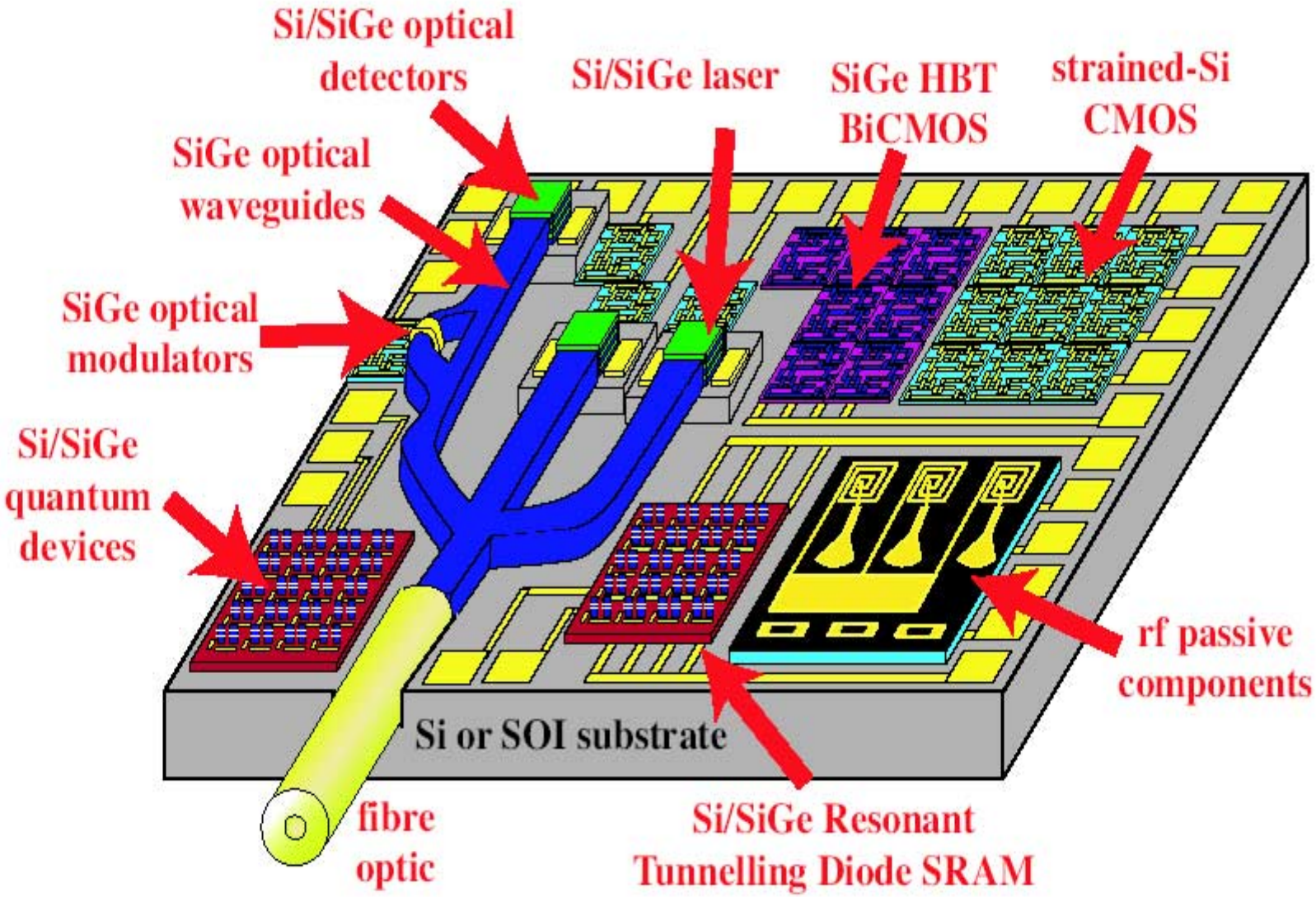
4. CVD Equipment for SiGe

5. Device aplications and commercialization

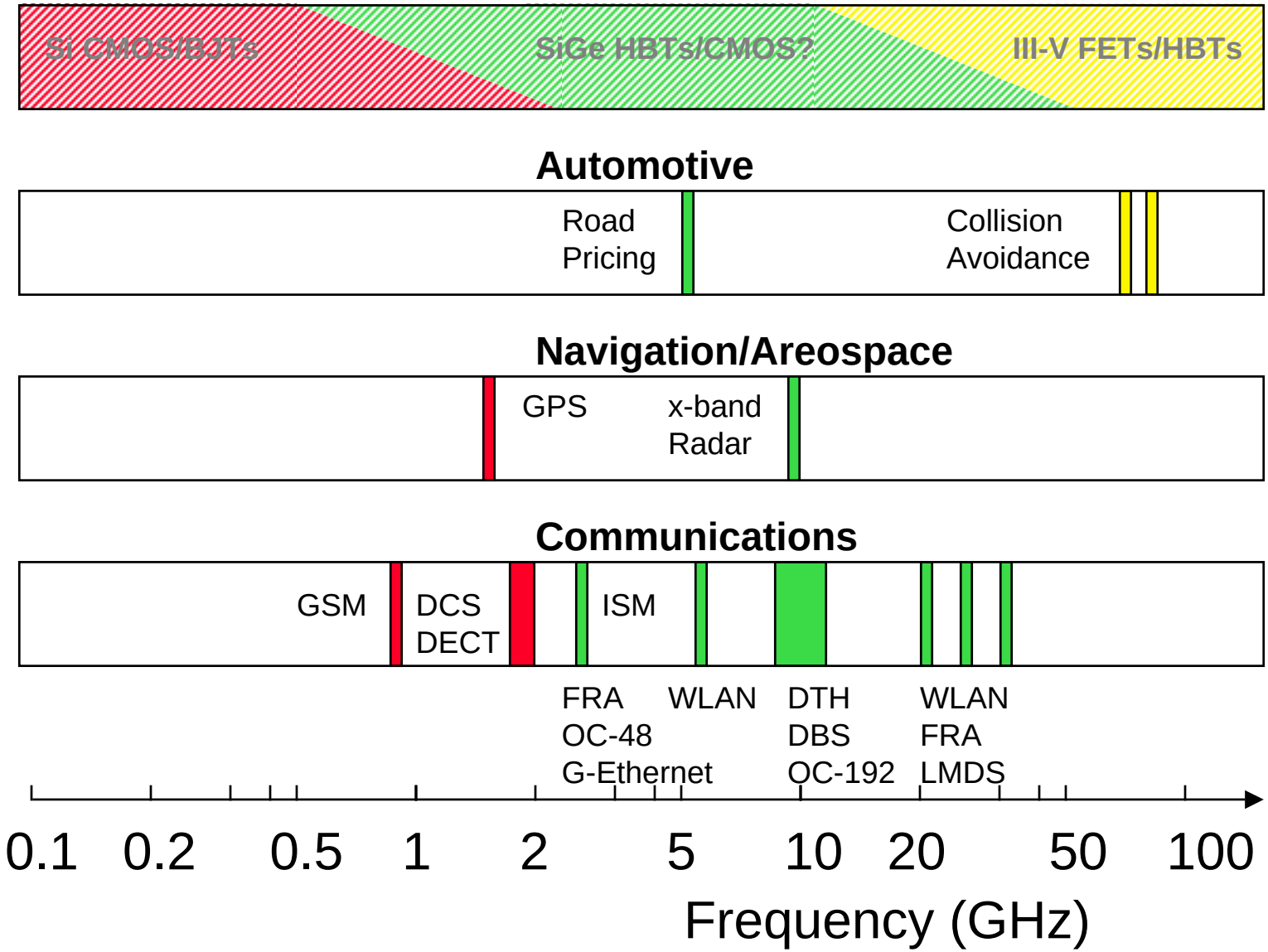
6. SiGe materials engineering, metrology

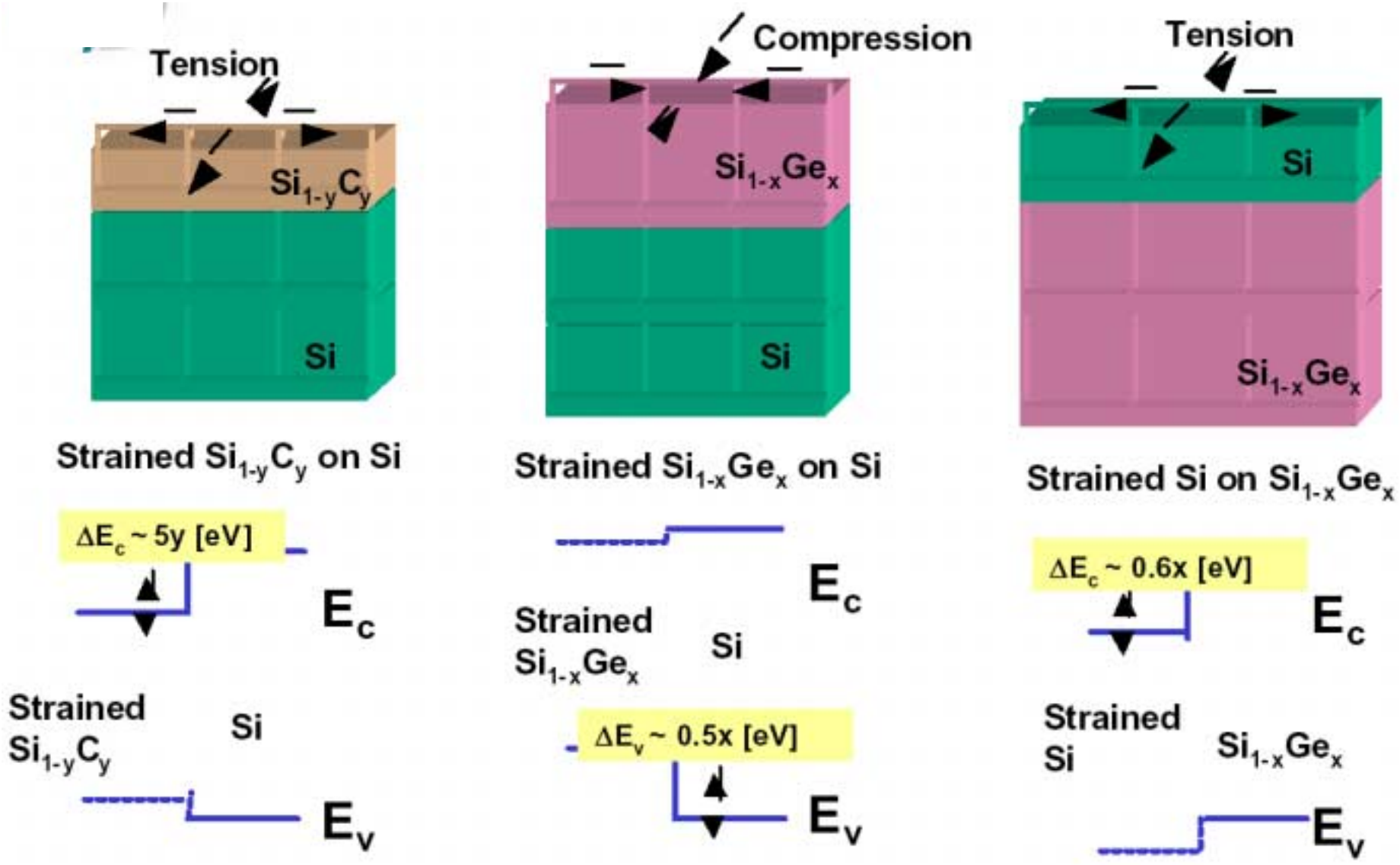
7. Summary and Discussion


EMITTER
COLLECTOR
BASE
CONTACT
1 cm
GERMANIUM
SUBSTRATE

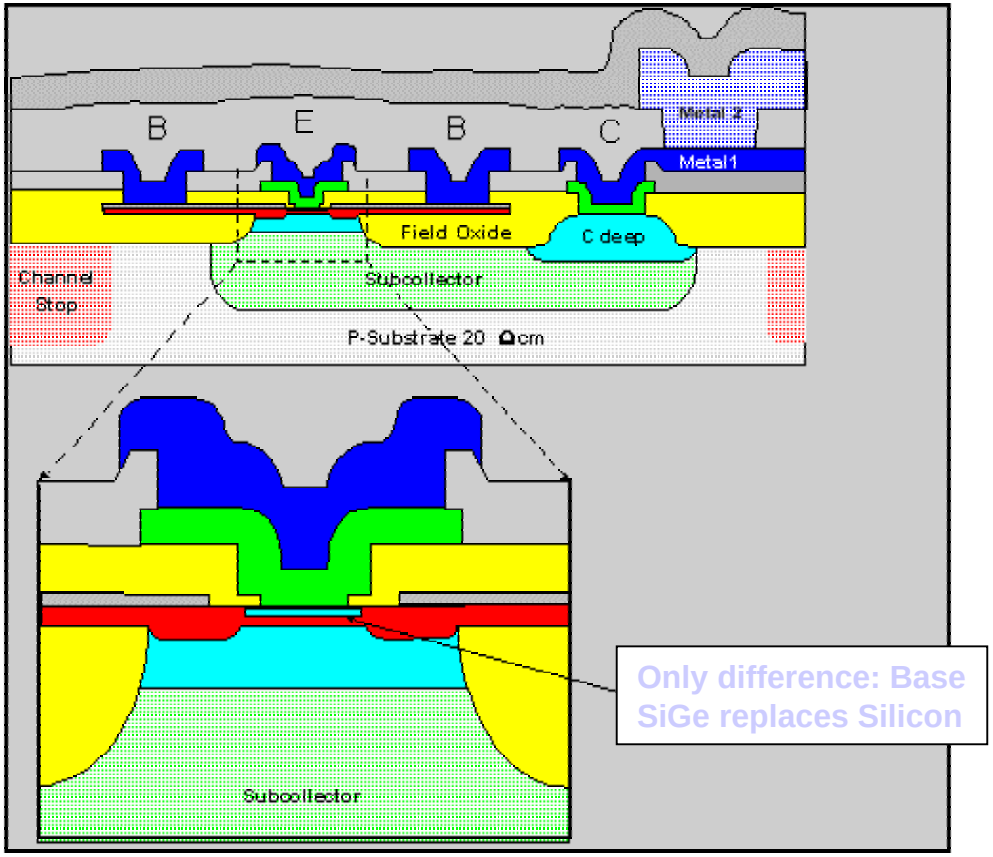

Si/SiGe optical detectors
Si/SiGe laser
SiGe HBT BiCMOS
strained-Si CMOS
SiGe optical waveguides
SiGe optical modulators
Si/SiGe quantum devices
rf passive components
Si or SOI substrate
fibre optic
Si/SiGe Resonant Tunnelling Diode SRAM

SiGe's Market Opportunity...




Tension
$Si_{1-y}C_y$
Si
Strained $Si_{1-y}C_y$ on Si
$\Delta E_c \sim 5y$ [eV]
E_c
Strained $Si_{1-y}C_y$
Si
E_v
Compression
$Si_{1-x}Ge_x$
Si
Strained $Si_{1-x}Ge_x$ on Si
E_c
Strained $Si_{1-x}Ge_x$
Si
$\Delta E_v \sim 0.5x$ [eV]
E_v
Tension
Si
$Si_{1-x}Ge_x$
Strained Si on $Si_{1-x}Ge_x$
$\Delta E_c \sim 0.6x$ [eV]
E_c
Strained Si
$Si_{1-x}Ge_x$
E_v

SiGe HBT device structure and process description

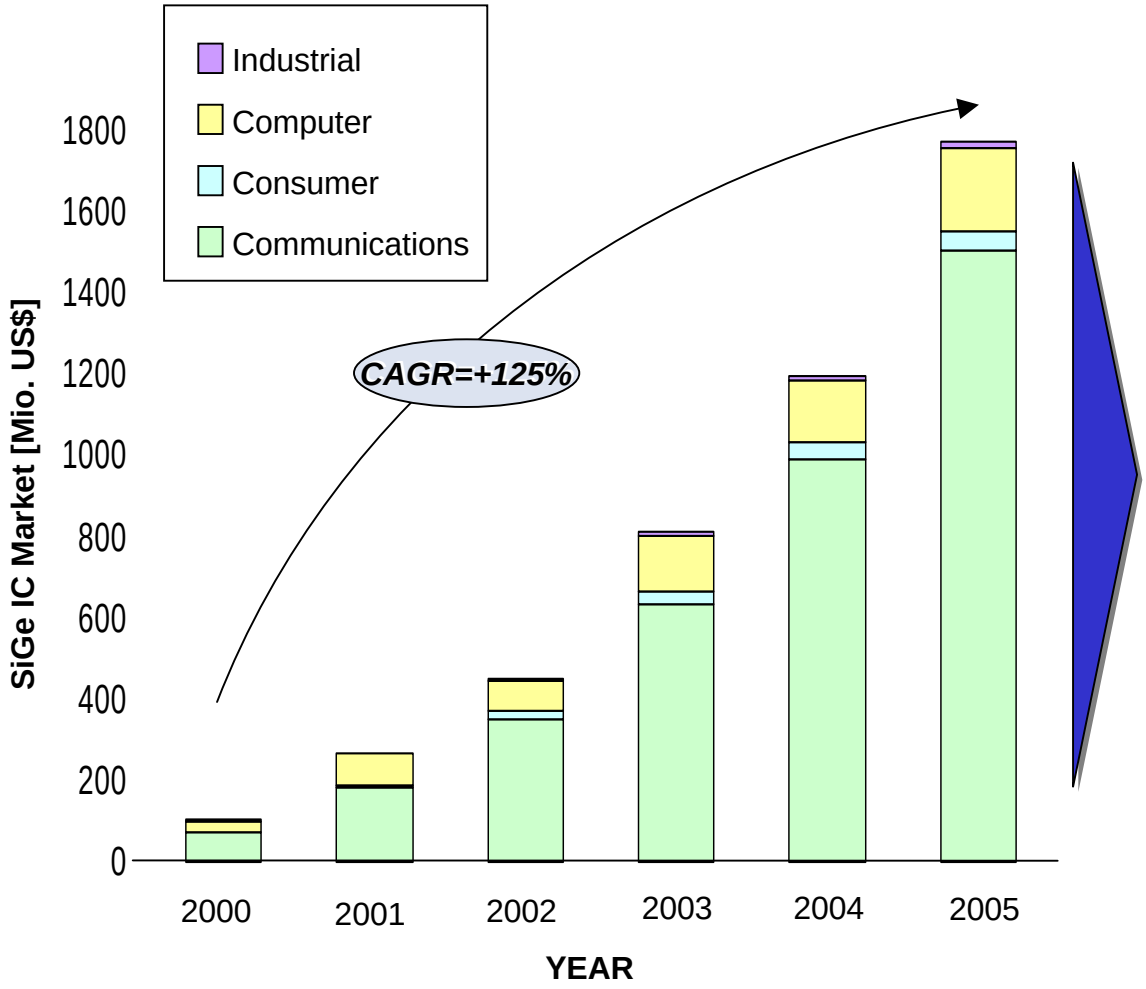


Key figures of SiGe HBT process

- SiGe BiCMOS uses SiGe HBT + Si CMOS
- SiGe HBT shows same process as Si BT with exception of 30-80 nm thin SiGe base layer (Ge <25%)
- Growth rates used are about 30 nm/min (~ 2 min for base layer)
- Typically, same LPCVD growth chambers can deposite both Si and SiGe layers
- Depending on SiGe HBT process, base layer deposited either using selective or differential epitaxy

SiGe‘s main market is telecommunication (wireless and datacom)

SiGe IC forecast by market, 2000 to 2005, in mil. US$



Comments

- **SiGe viable alternative to GaAs**
- Main markets being targeted:
  - Cellular / Cordless / WLAN
  - FO-Datacom (MUX/DEMUX)
  - PC interface cards / LAN
- Future trends:
  - integrated low power RF-front end of most handsets
  - First choice for up/down conversion in tuners/ transceivers
  - will dominate 40 Gbps

Source: Strategies Unlimited, 1999

CAGR: Compound Average Growth Rate

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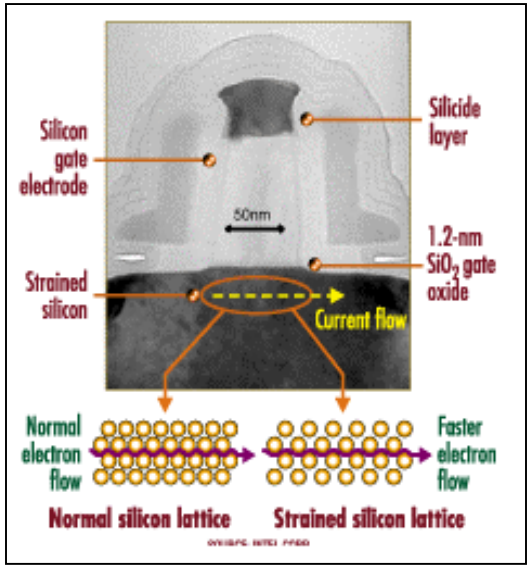
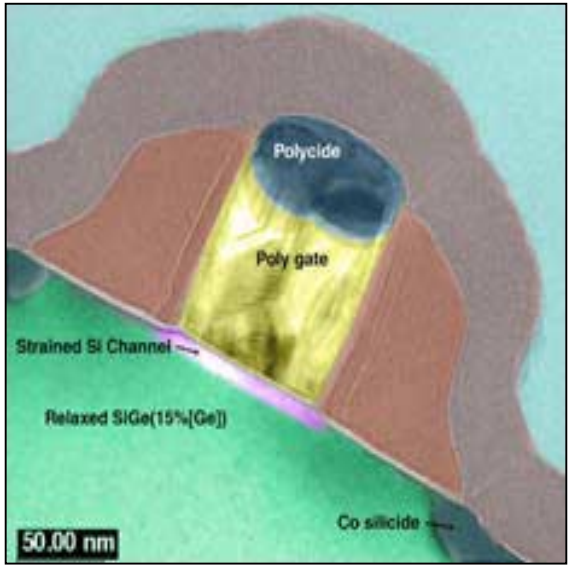
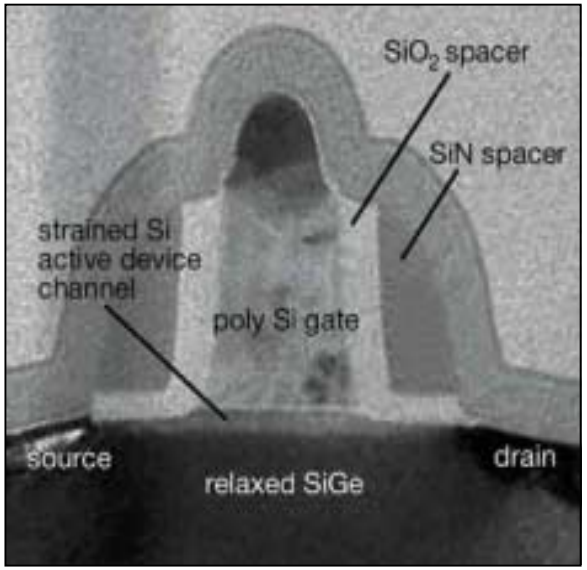
Strained Si: prototypes from Intel, IBM & UMC demonstrated

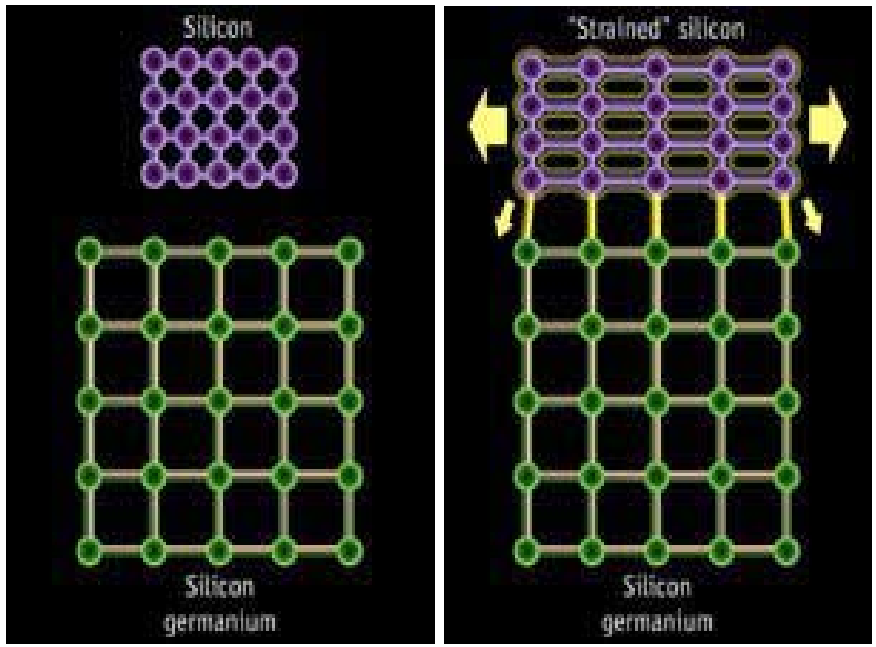






Almost all large Si-CMOS manufacturers are presenting cross sectional pictures of CMOS transistors (with gate lengths between 65 and 90 nm) which use Strained-Si technology. Intel and IBM use their own technology, whereas UMC is Amberwave's licensee

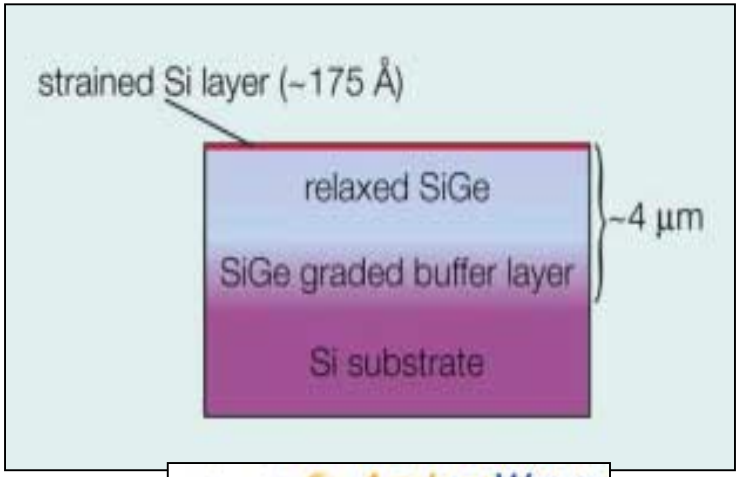
Strained-Si HeteroWafer® technology: process and actual status

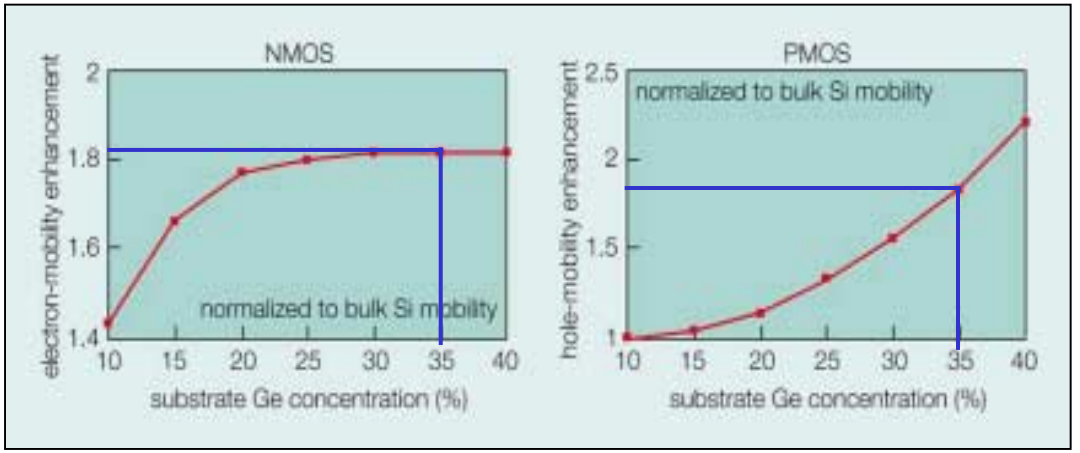


Actual status Strained-Si process

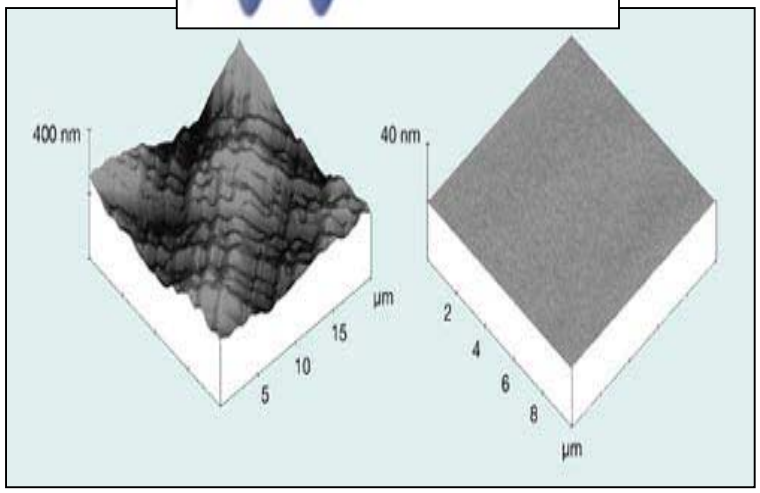
- Strained Si technology enables improvement in CMOS performance and functionality via replacement of the bulk, cubic-crystal Si substrate with a Si substrate that contains a tetragonally distorted, biaxially strained Si thin film at the surface
- Different types of processes developed and patented by the main players: Amberwave (IQE) - AIXTRON, IBM,Toshiba & Intel
- First demos of perfect working 52 Mbit SRAMs with 90 nm CMOS devices on 300 mm wafers available from Intel. Ramp-up of Pentium 4 production with Str.-Si planned for 2H/2003 !
- Process and substrate costs still not 100% fixed. Price expectations for substrate from IC manufacturers still unknown

Strained Si process of Amberwave: One of the Strained Si pioneers



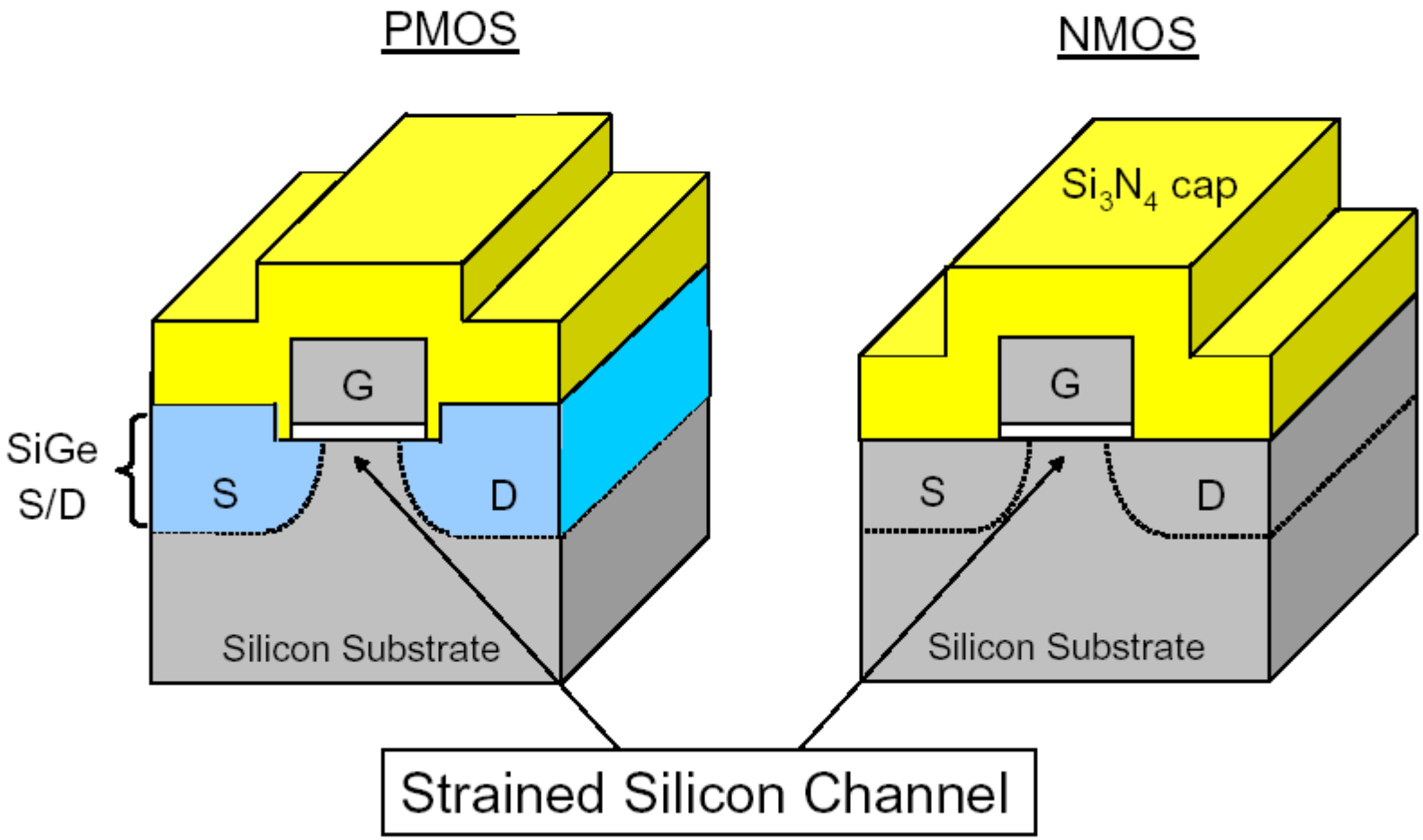


AmberWave SYSTEMS

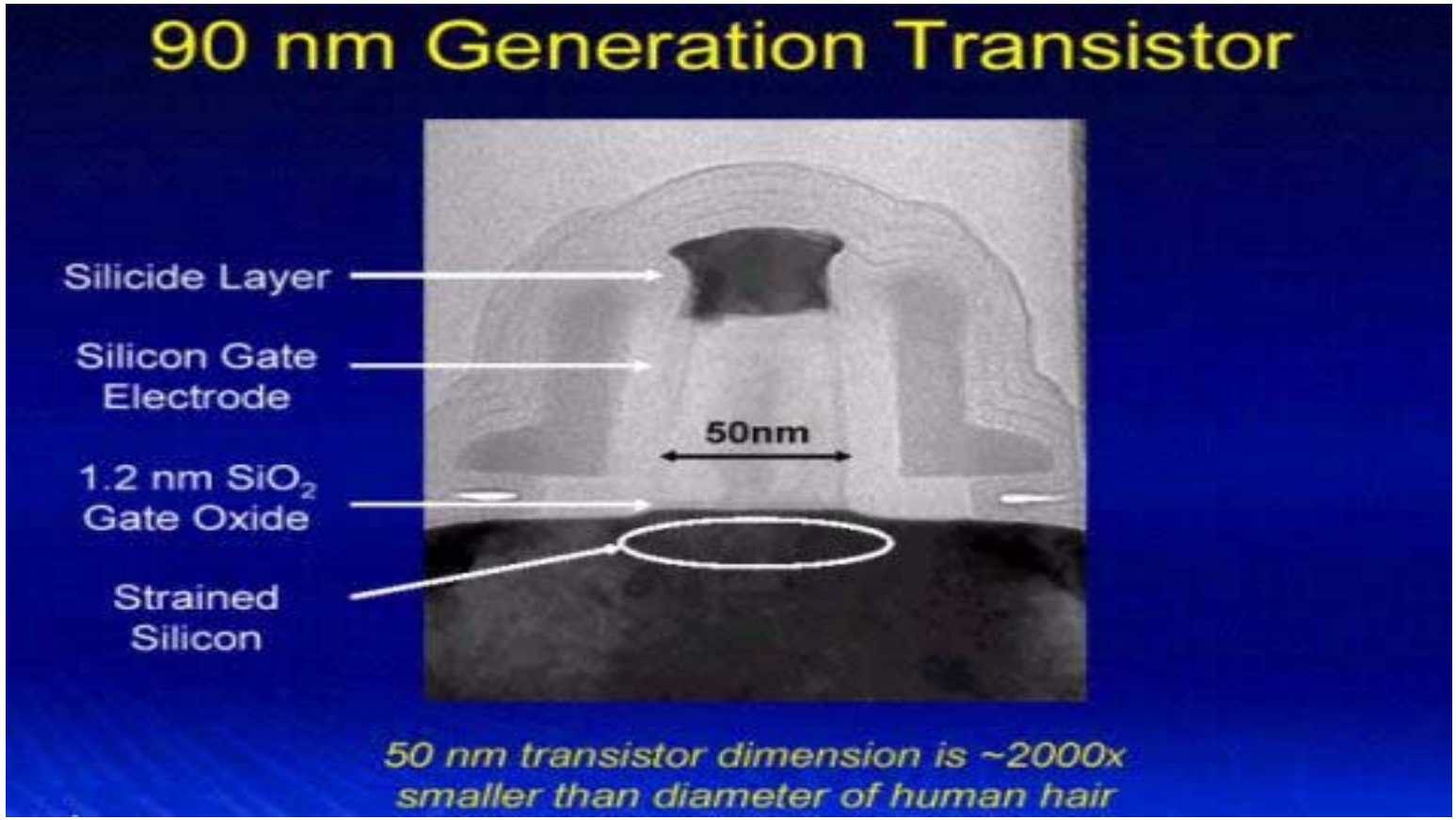


- Typically, 2 to 4 µm thick graded SiGe buffer layer, followed by thin (<20 nm) strained Si channel layer
- Depending on substrate Ge concentration, clear mobility and transistor current drive improvement
- Through Amberwave's proprietary chemical-mechanical polishing (CMP) intermediate process, SiGe buffer layer surface roughness is eliminated before Si layer deposi-tion, resulting in same quality compared to bulk Si wafers

Intel's Strained Silicon Transistors

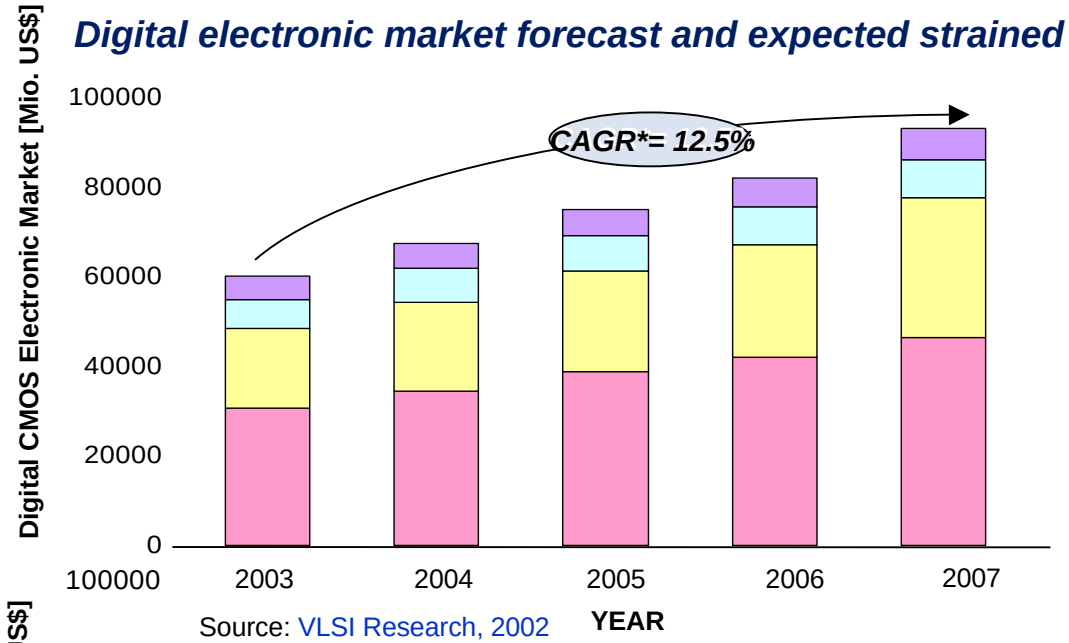


Strained Silicon CMOS technology
*SiGe deposited selectively,
Intel Pentium IV in production

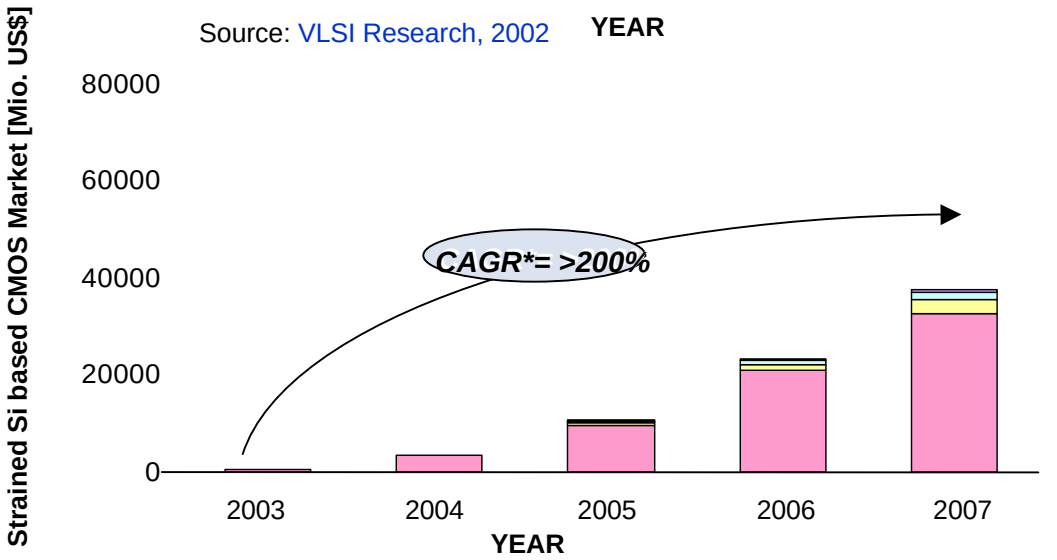


Strained silicon mainly addresses high-end digital CMOS markets

Digital electronic market forecast and expected strained Si penetration, 2003 to 2007, in mil. US$



Source: VLSI Research, 2002



Source: AIXTRON estimates

- Si FPGAs
- Si Digital Signal Processors (DSPs)
- Si Micro-controllers (MCUs)
- Si Microprocessors (MPUs)

Assumptions

- Main application will be high-end Microprocessors like IBM‘s Power-PC, SUN‘s Sparc, AMD‘s Athlon, Intel Pentium / Itanium.
- Main markets being targeted: PCs, workstations, game consoles, other internet appliances
- Future trends: Strained Si penetrates 3G/WLAN wireless applications (DSPs/MCUs)

CAGR: Compound Average Growth Rate

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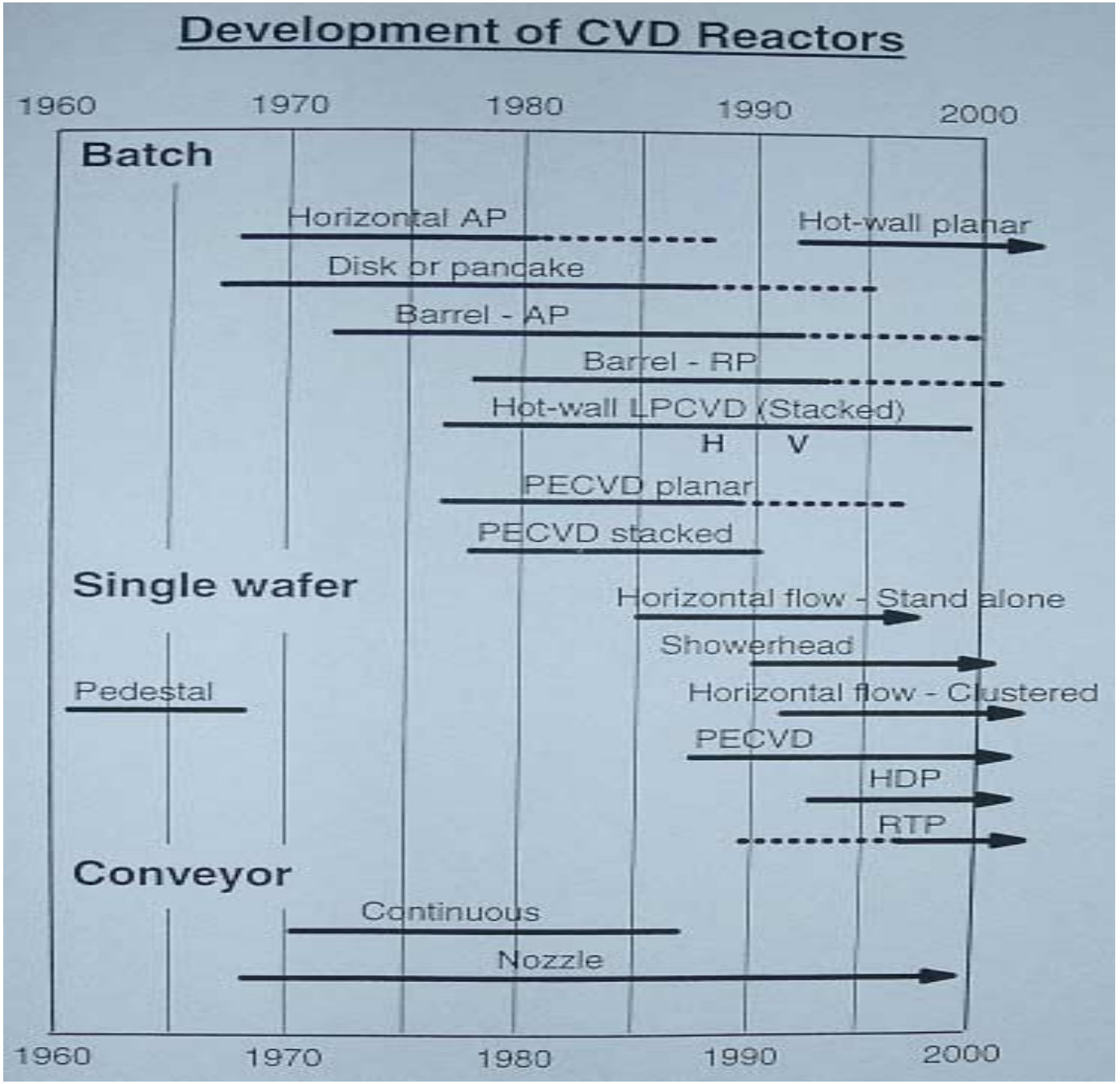
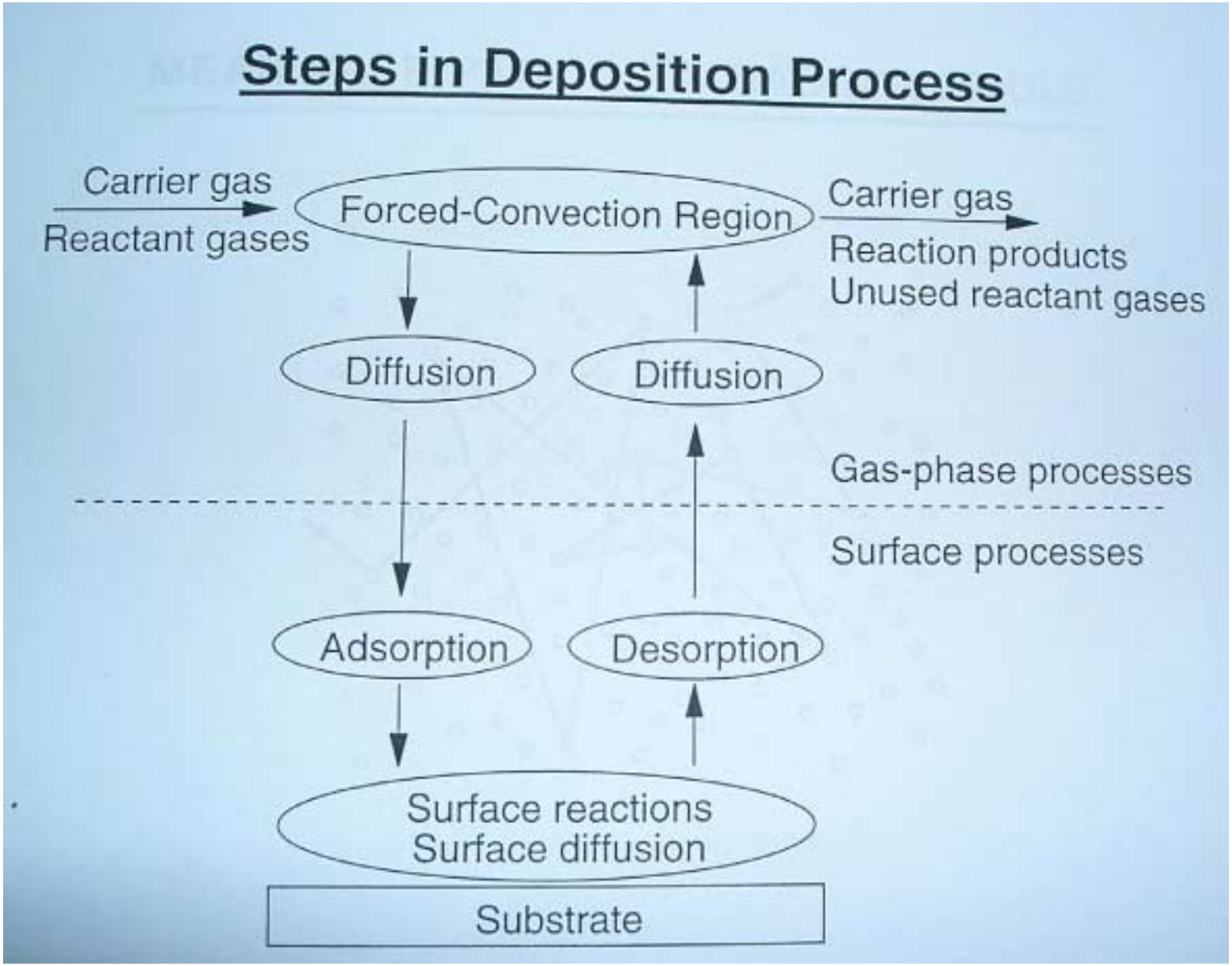
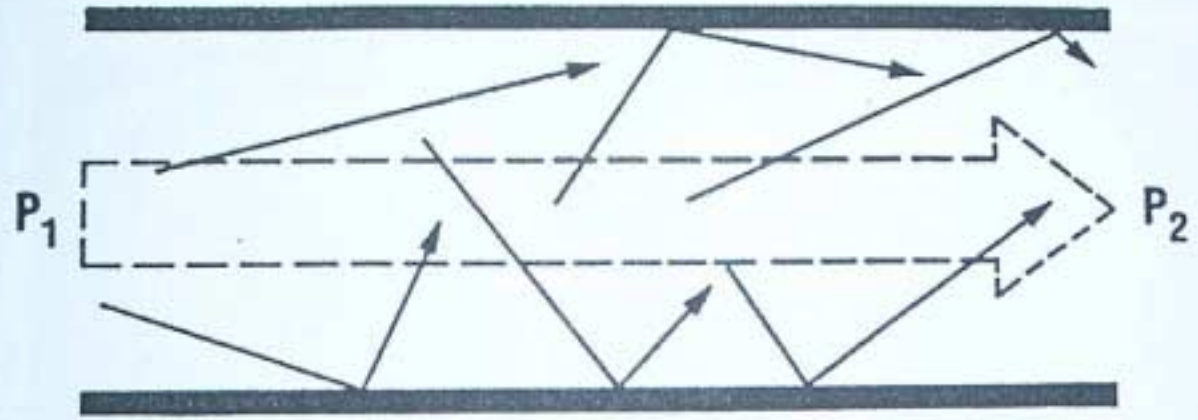

Development of CVD Reactors
1960
1970
1980
1990
2000
Batch
Horizontal AP
Hot-wall planar
Disk or pancake
Barrel - AP
Barrel - RP
Hot-wall LPCVD (Stacked)
H
V
PECVD planar
PECVD stacked
Single wafer
Horizontal flow - Stand alone
Showerhead
Pedestal
Horizontal flow - Clustered
PECVD
HDP
RTP
Conveyor
Continuous
Nozzle
1960
1970
1980
1990
2000

Steps in Deposition Process

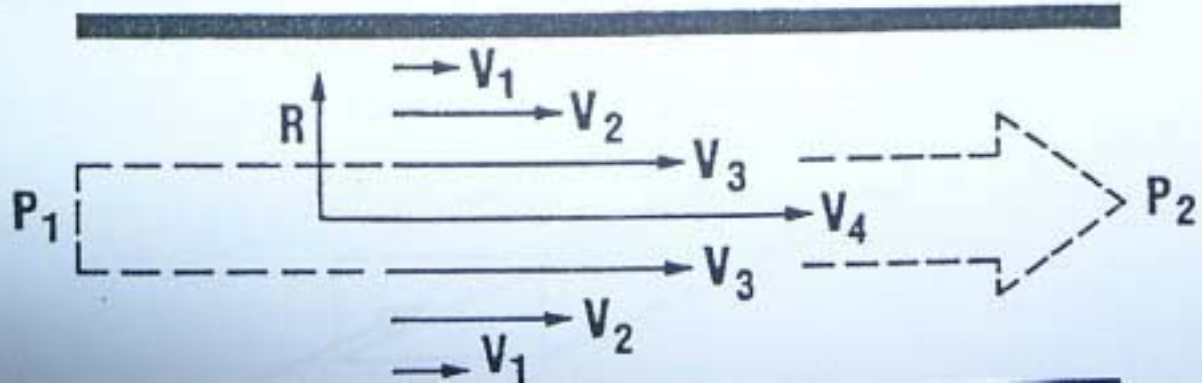


DISTRIBUTION OF MOLECULAR VELOCITIES

Molecular Flow in a Tube

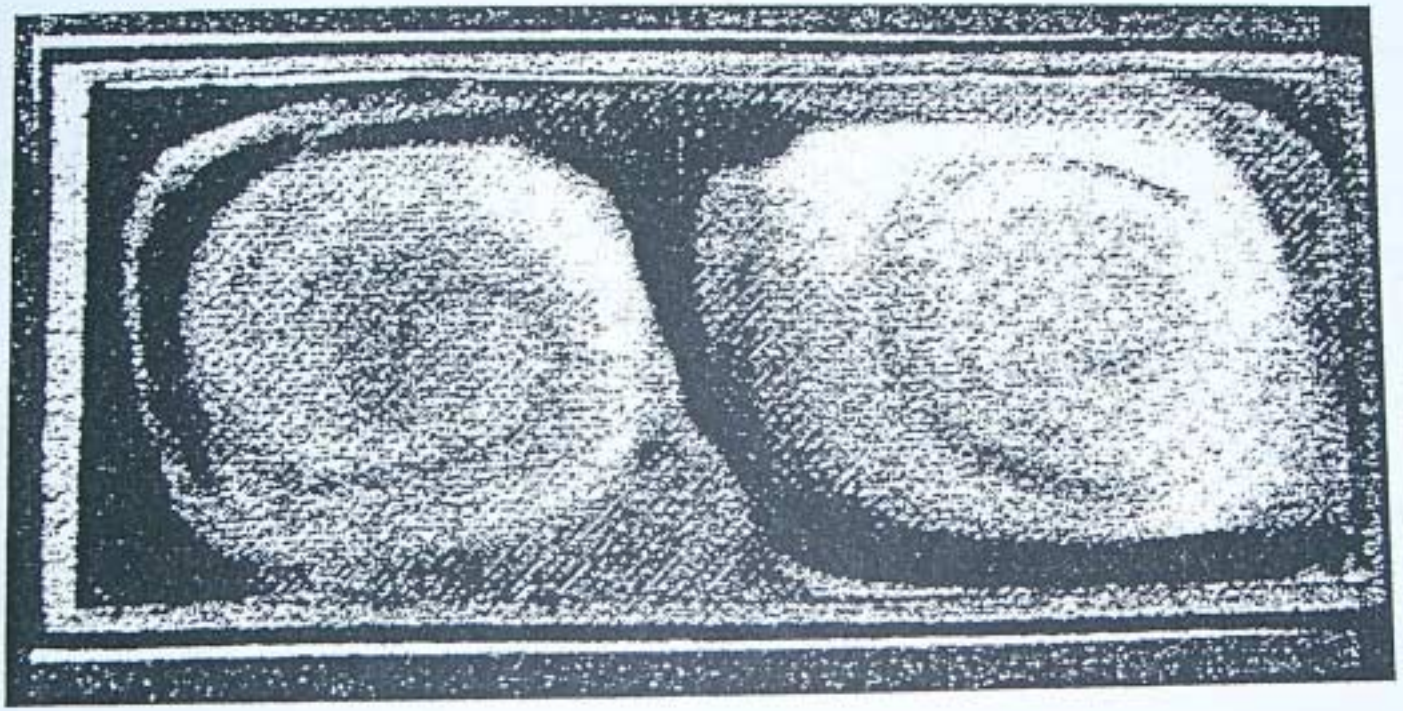


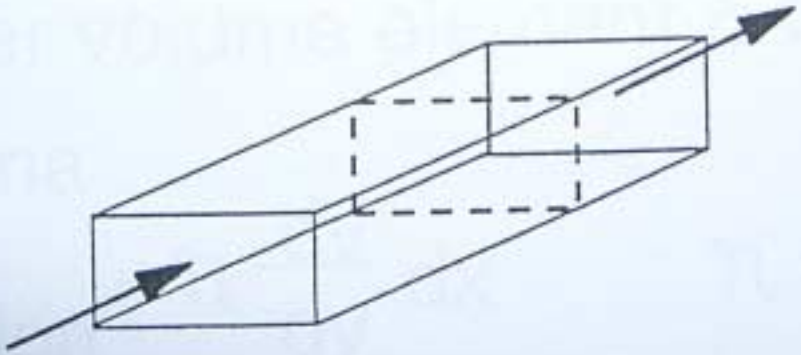
Viscous Flow in a Tube



Free Convection

Cross Section of Rectangular Chamber





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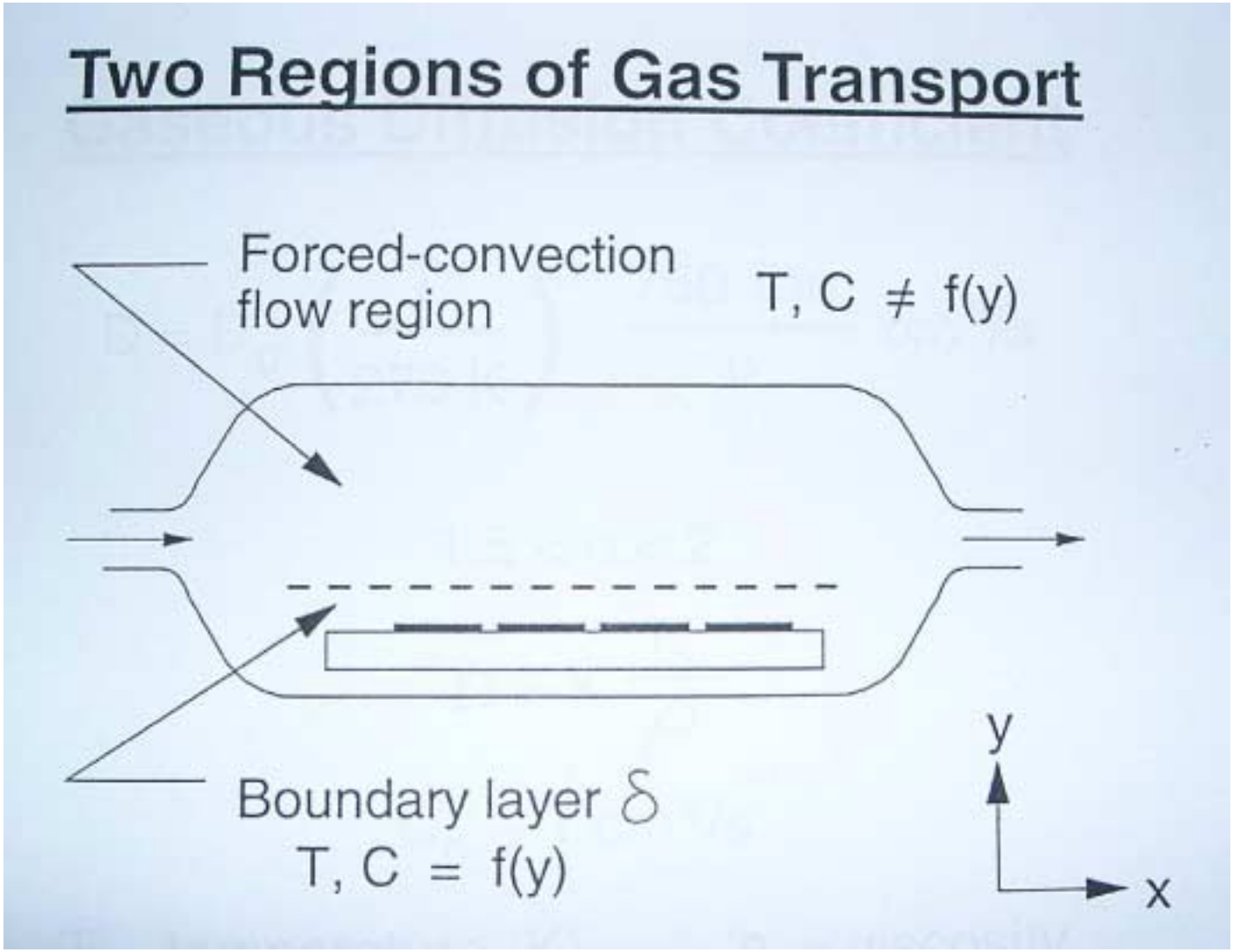
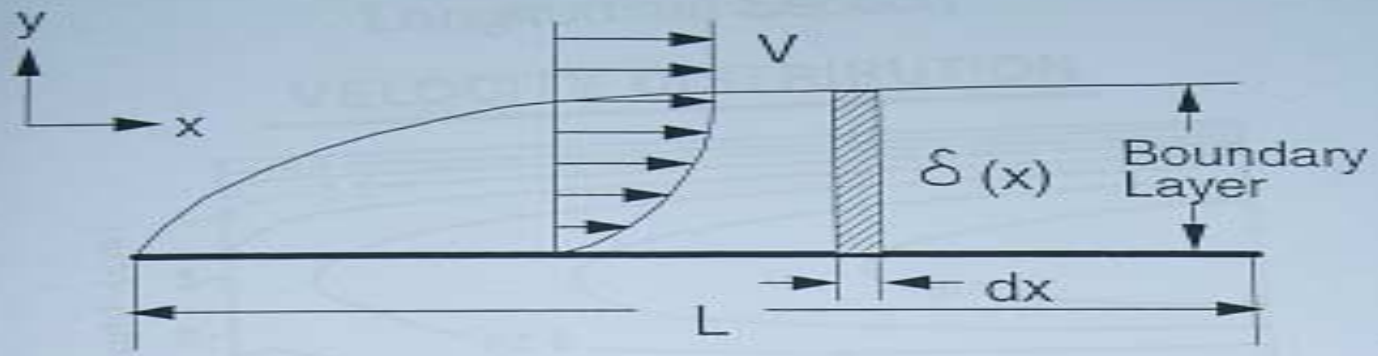
Two Regions of Gas Transport



Forced Convection

Development of Boundary Layer



Consider volume element $\delta\, dx$

$$F = ma$$

$$F_{friction} = \eta \frac{dv}{dy} dx \qquad \eta = \text{viscosity}$$

$$m = \rho \delta\, dx \qquad \rho = \text{density}$$

$$a = \frac{dv}{dt} = \frac{dv}{dx}\frac{dx}{dt} = \frac{dv}{dx} v$$

$$\eta \frac{dv}{dy} dx = \rho \delta\, dx \frac{dv}{dx} v$$

Replacing differentials by differences

$$\eta \frac{V}{\delta} \approx \rho \delta \frac{V}{x} V$$

V - velocity

$$\delta(x) = \sqrt{\frac{\eta\, x}{\rho\, V}}$$

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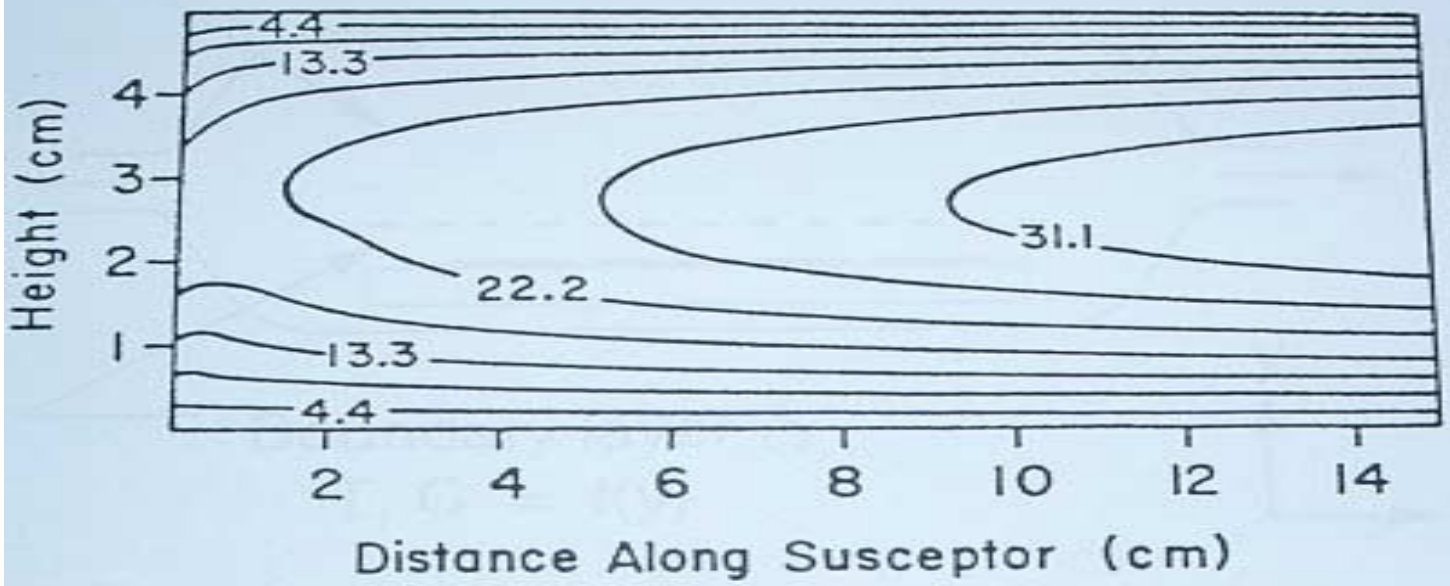
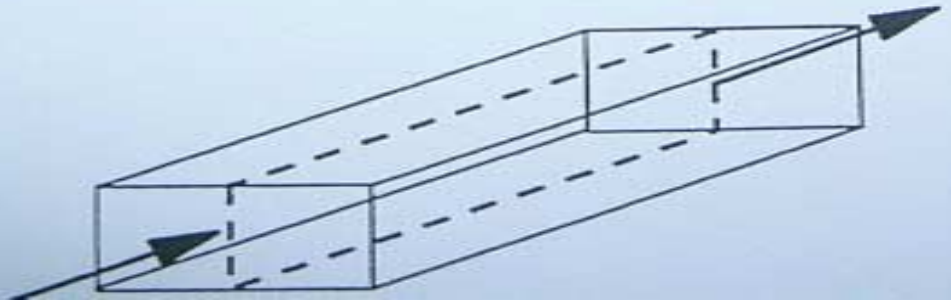
Boundary Layer

Longitudinal Section

VELOCITY DISTRIBUTION



M E Coltrin, R J Kee, and J A Miller, J. Electrochem. Soc. 131, 425 (February 1984)



Deposition Kinetics (1)

Diffusion and Surface Reaction

Diffusion Through Boundary Layer

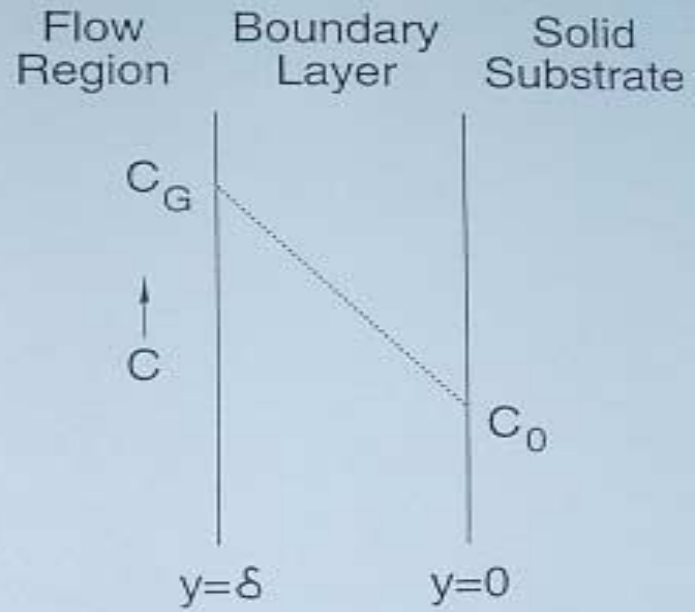
$$F_1 = D \frac{C_G - C_0}{\delta}$$

Reaction at Surface (y=0)

$$F_2 = k C_0$$

Steady State: $F_1 = F_2$

$$C_0 = \frac{C_G}{1 + k\delta/D}$$



F_1 = Flux of reactant diffusing through boundary layer

F_2 = Flux reacting at surface

δ = Boundary-layer thickness

C_G = Reactant concentration in forced-convection region

C_0 = Reactant concentration adjacent to surface

D = Gaseous diffusion coefficient

k = Reaction rate coefficient

Deposition Kinetics (3)

Diffusion-Limited Region

Increase Temperature

$$k = k_o \exp(-E_a/kT)$$

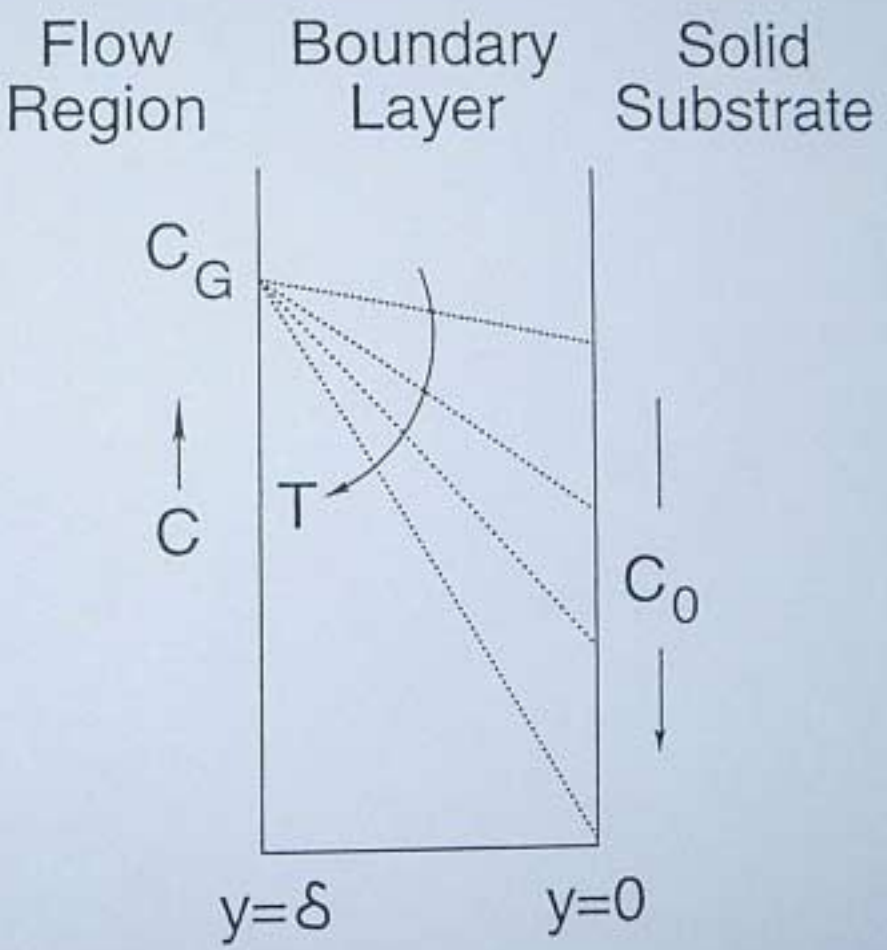
Fast Surface Reaction

Slow Diffusion

$$C_0 = \frac{C_G}{1 + k\delta/D}$$

$$C_0 \approx 0$$

Diffusion or *Mass-Transport Limited Region*



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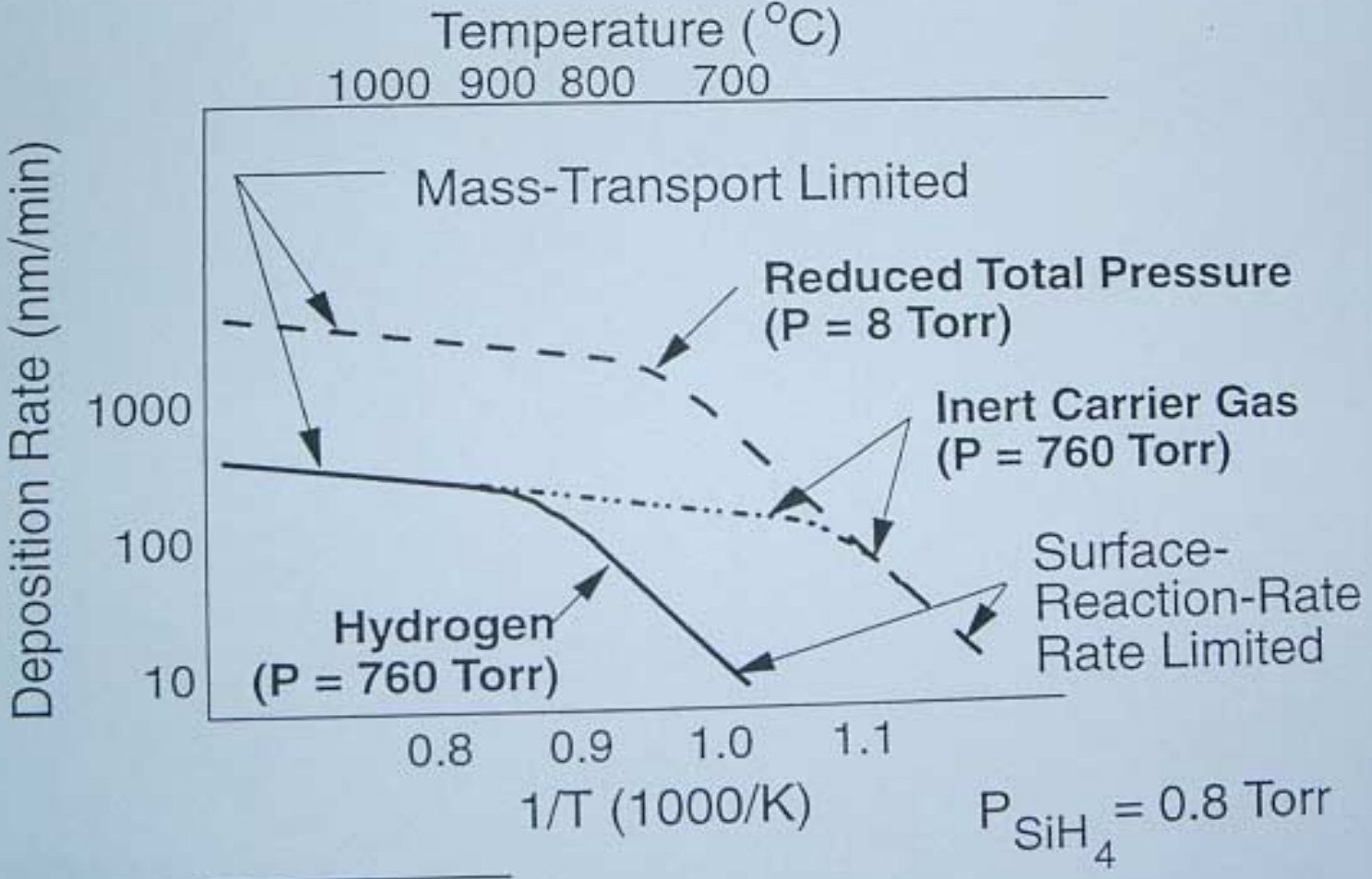
Effect of Carrier Gas and Pressure on Deposition Rate

$$SiH_4 \rightarrow Si + 2H_2$$



W.A.P. Claassen and J. Bloem,
Philips J. Res. 36, 122 (1981)

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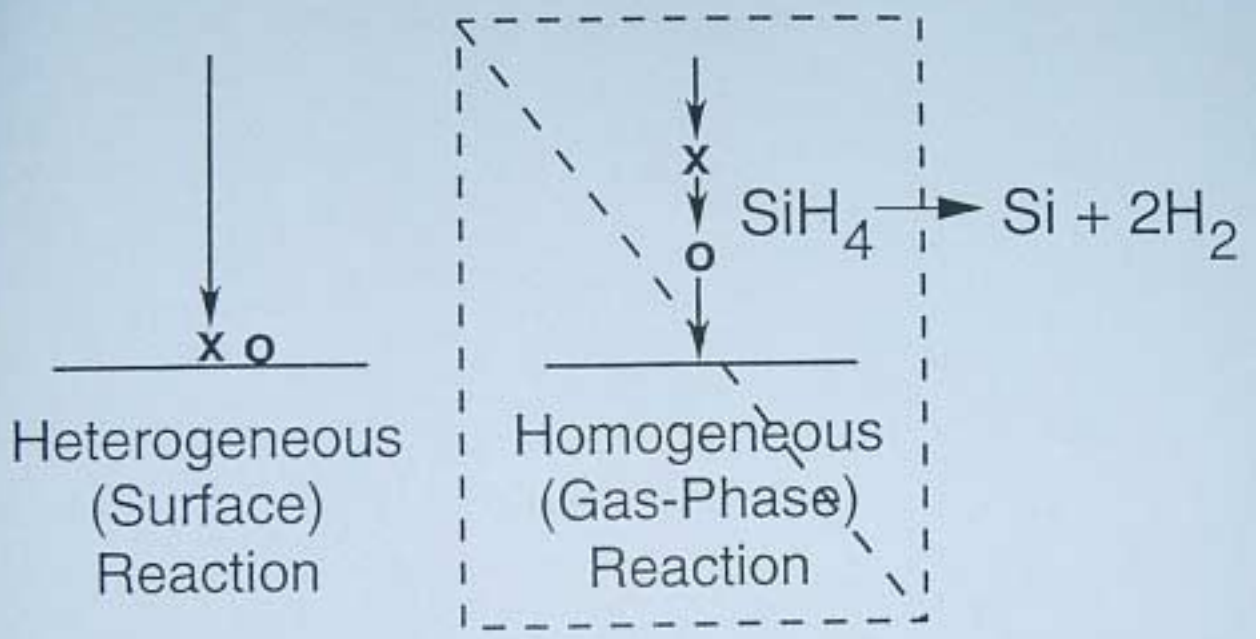
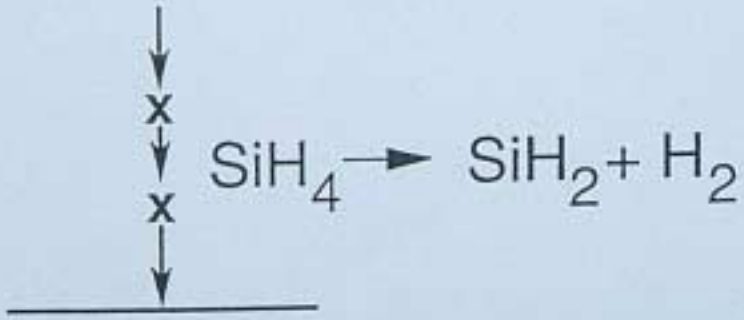
Gases for Silicon Epitaxy

	Silane (SiH_4)	Dichlorosilane (SiH_2Cl_2)	Silicon Tetrachloride ($SiCl_4$)
Temperature	1000-1050°C	1050-1100°C	1150-1200°C
Reaction	$SiH_4 \rightarrow Si + 2H_2$	$SiH_2Cl_2 \rightarrow Si + 2HCl$	$SiCl_4 + 2H_2 \rightarrow Si + 4HCl$
Reversible	No	Yes	Yes
HCl Byproduct	No	Yes	Yes
Gas-Phase Nucleation	Yes	No	No
Deposition Rate	0.2 μm/min	~1 μm/min	>2 μm/min
Flow Control	Easy	Moderate	Difficult
Cost	High	Moderate	Low
Danger	High	Moderate	Moderate
Used for	Thinner Layers	Many Layers	Thicker Layers

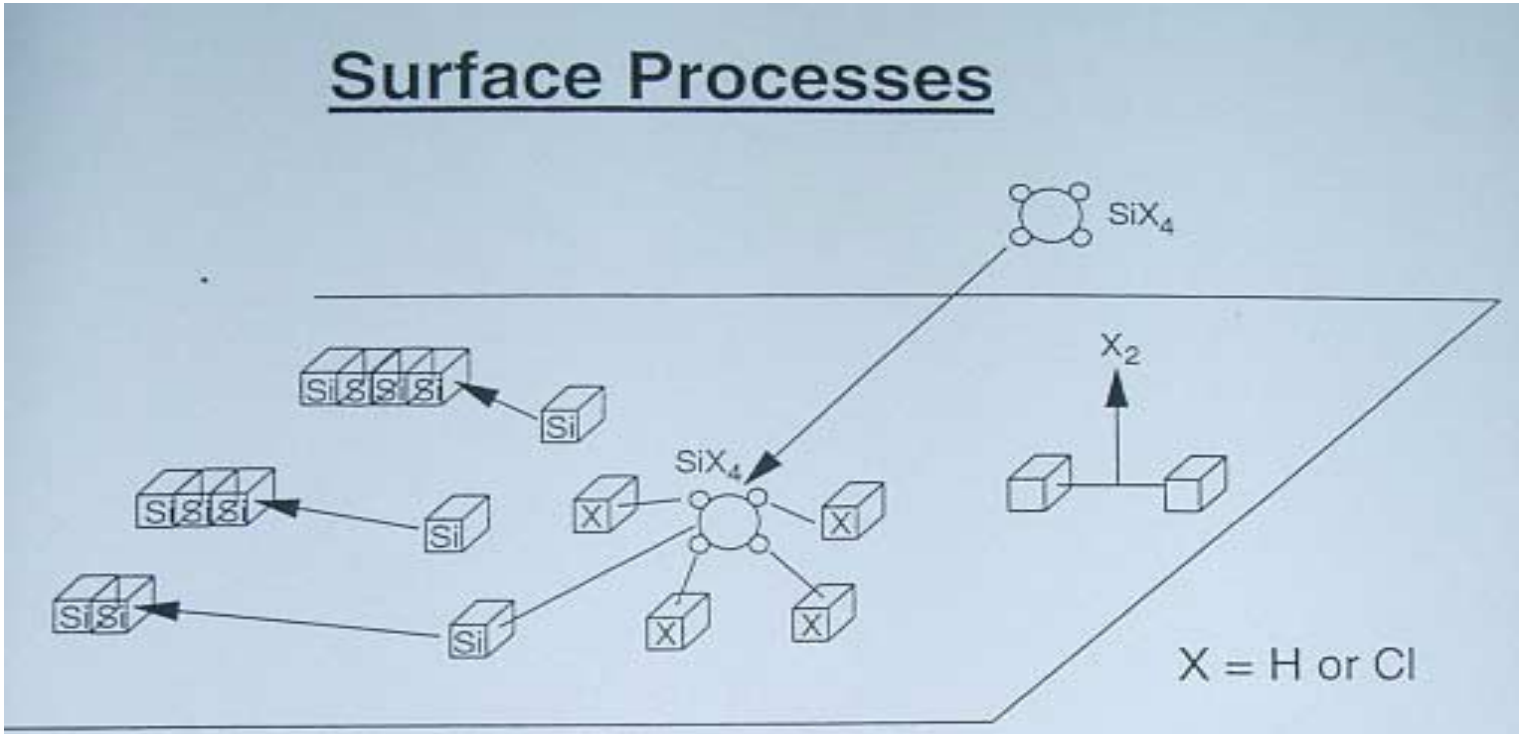
Surface Reaction





Gas-Phase Reaction
To Intermediate
Gas-Phase Species is OK

Surface Processes



- Impingement
- Surface adsorption
- Surface diffusion
- Chemical reaction
- Surface diffusion
- Nucleation
- Incorporation
- Byproduct desorption

Structure Depends on Surface Diffusion

- Deposition temperature
- Deposition rate

$$L \approx \sqrt{D\,t} \sim \frac{1}{\sqrt{R_D}} \exp\left(\frac{-E_a}{2kT}\right)$$

L= surface diffusion length

D = Surface diffusion coefficient

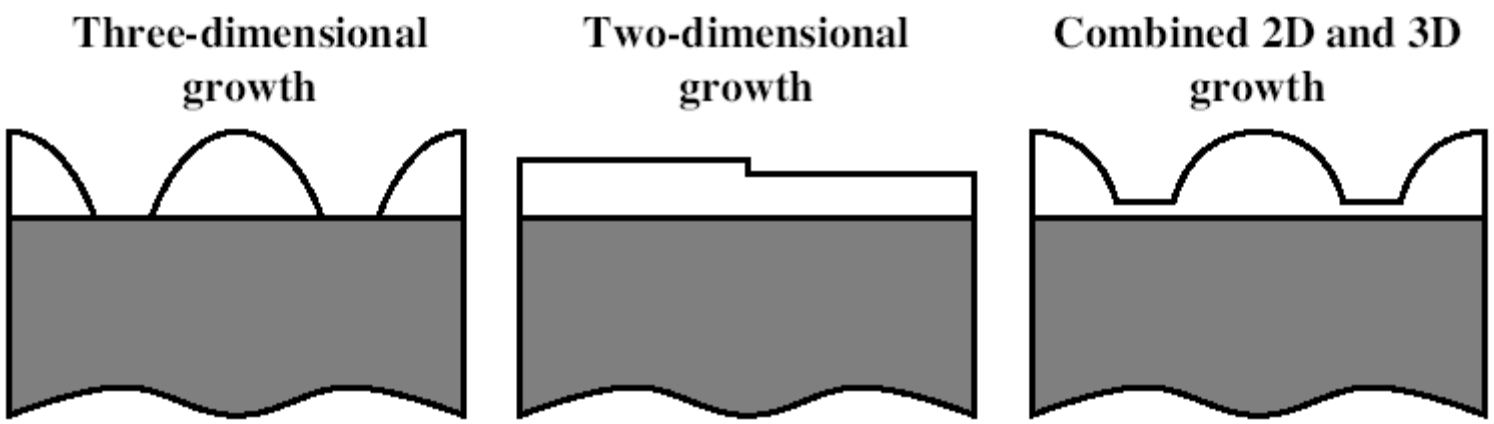
t = time available for surface diffusion

R_D = deposition rate

E_a = activation energy

- Deposition pressure

  Blocking of diffusion paths by adsorbed reactants, carrier gas, or impurities


Three-dimensional growth
Two-dimensional growth
Combined 2D and 3D growth

Deposition Rate and Available Surface Sites

Surface-reaction-limited region

$$R_{Adsorption} = Flux\ S_C\ n_{ss}\ \theta_F$$

$$R_{Reaction} = k\ n_{ss}\ \theta_{SiH_4}$$

$$\theta_F = 1 - \theta_{SiH_4} - \theta_H$$

$$R_D = \frac{k\ n_{ss}(1 - \theta_H)\ Flux}{k / (S_C) + Flux}$$

$$Flux \sim P_{SiH_4}$$

$$R_D = \frac{A\ P_{SiH_4}}{1 + B\ P_{SiH_4}}$$

S_C = (Reactive) sticking coefficient

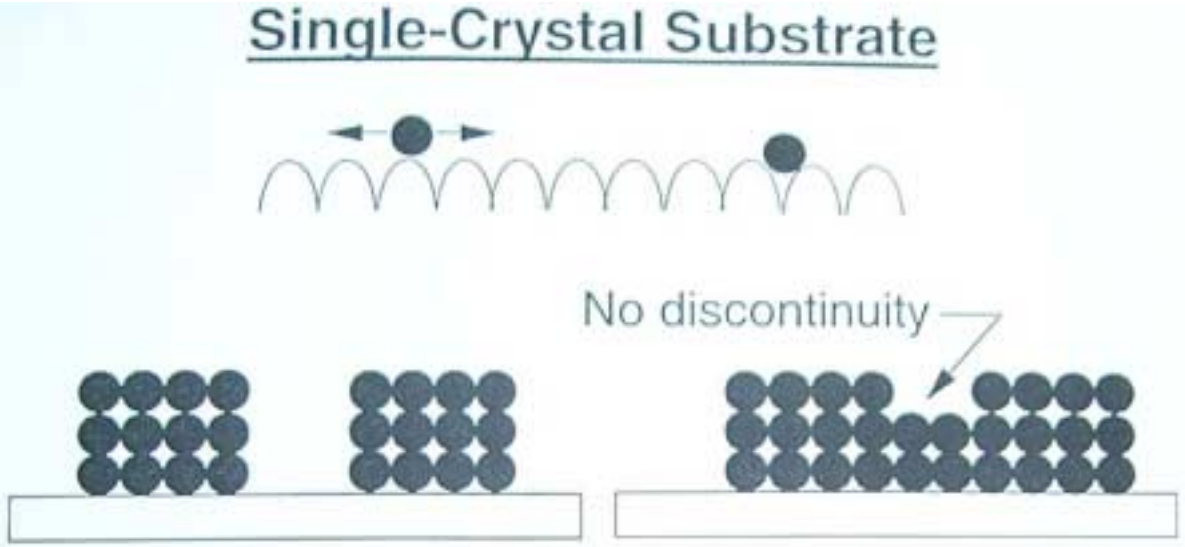
n_{ss} = Total number of surface sites

θ = Fraction of surface sites free (F) or covered with H or SiH_4

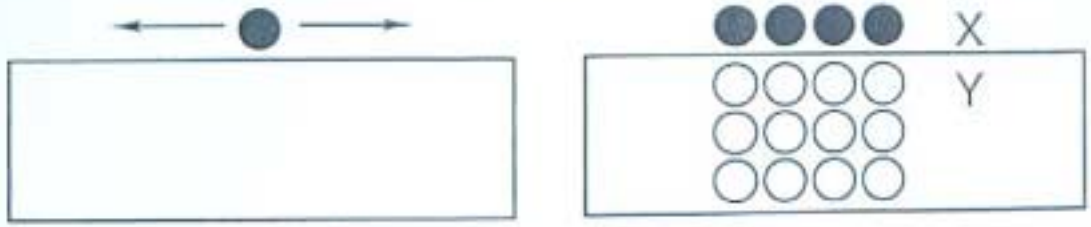
k = Reaction-rate coefficient

M L Hitchman, J. Kane, and A E Widmer, Thin Solid Films 59, 231 (1979)

Single-Crystal Substrate



Epitaxy



Isoepitaxy
Homoepitaxy
} X = Y

Heteroepitaxy: X ≠ Y

Unstrained if $a_X = a_Y$

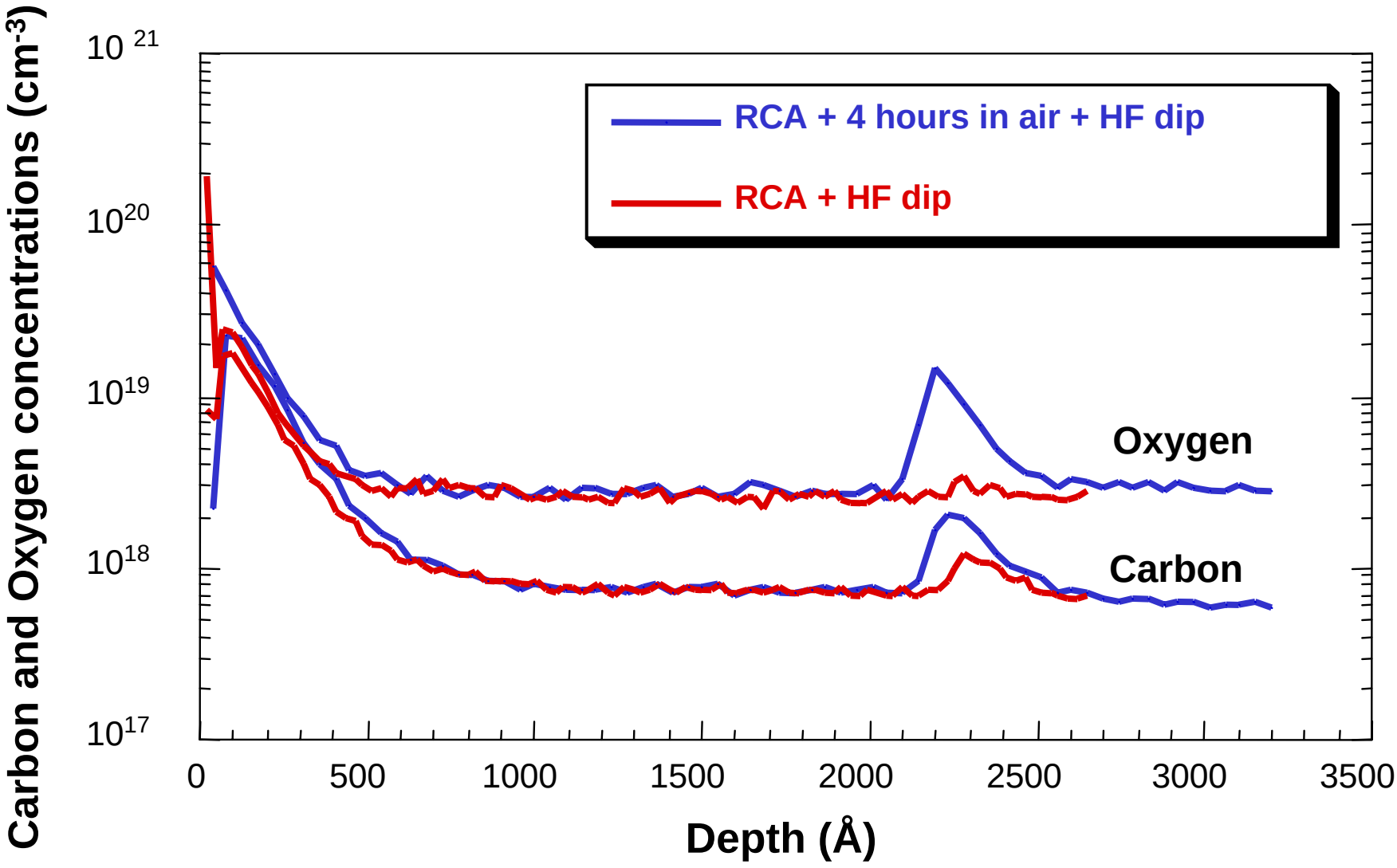
Strained if $a_X \neq a_Y$

(a = lattice constant)

Wafer Cleaning Before Epitaxial Deposition

- **Conventional:**
  - High temperature (1100-1250°C)
  - H_2 (+HCl)
- **Need:**
  - Low-temperature process (750-950°C)
- **Possibilities:**
  - Hydrogen-terminated surface
    - Minimizes native oxide formation
    - Dilute HF:H_2O etch *without* water rinse
      - Safety? Perhaps use cluster tool
    - Anhydrous or vapor HF?
      - Ex-situ?
      - Cluster tool?
  - Low-energy H_2 plasma?
  - UV-ozone?
  - ~~GeH_4?~~
- **Modification of conventional cleaning**
  - Use minimum safe water rinse time
  - Reduce oxygen concentration in rinse water

Effect of air exposure prior to HF passivation



Native Oxide Removal By High Temp. H_2 Bake

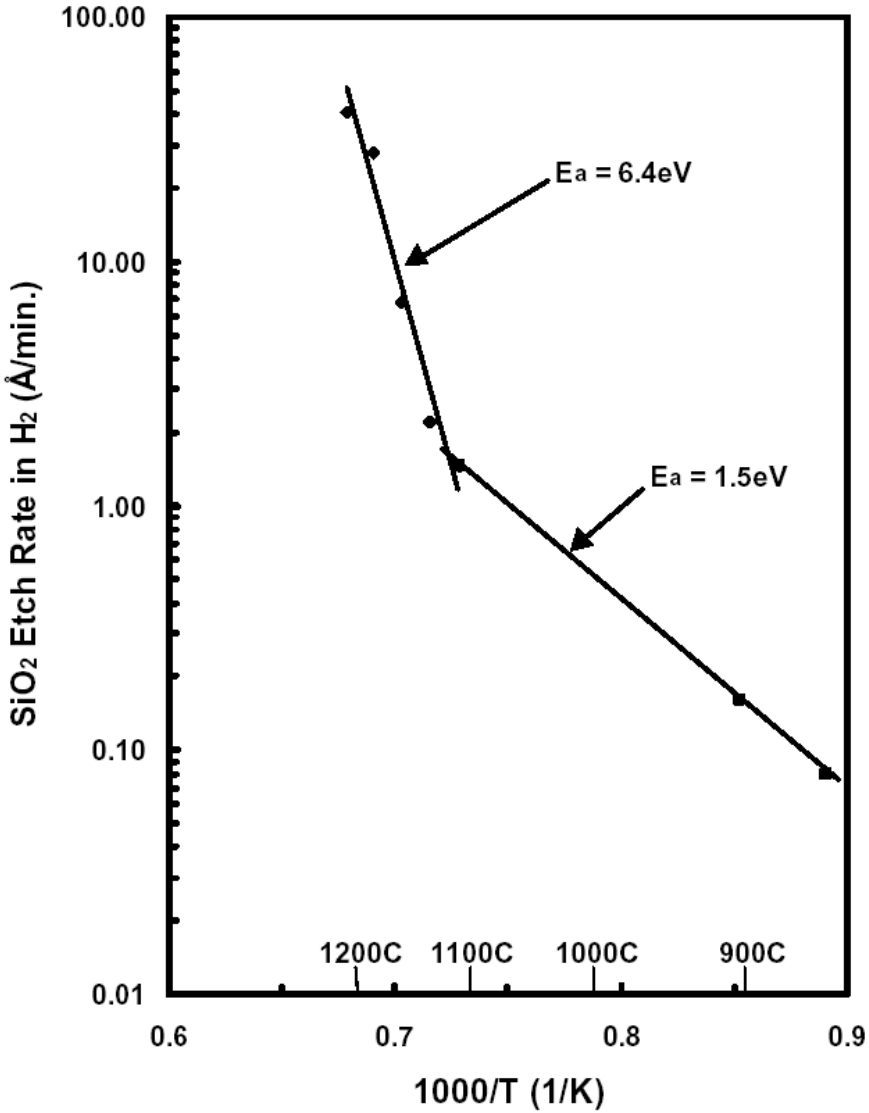
Traditional Production Si Epi Processes Use a High Temperature H_2 Bake to Remove Native Oxide by H_2 Reduction:

$$SiO_2(s) + H_2(v) \rightleftharpoons 2SiO(v) + H_2O(v)$$

The Native Oxide can also React Directly with the Si Surface:

$$SiO_2(s) + Si(s) \rightleftharpoons 2SiO(v)$$

But This Reaction is Self Limiting



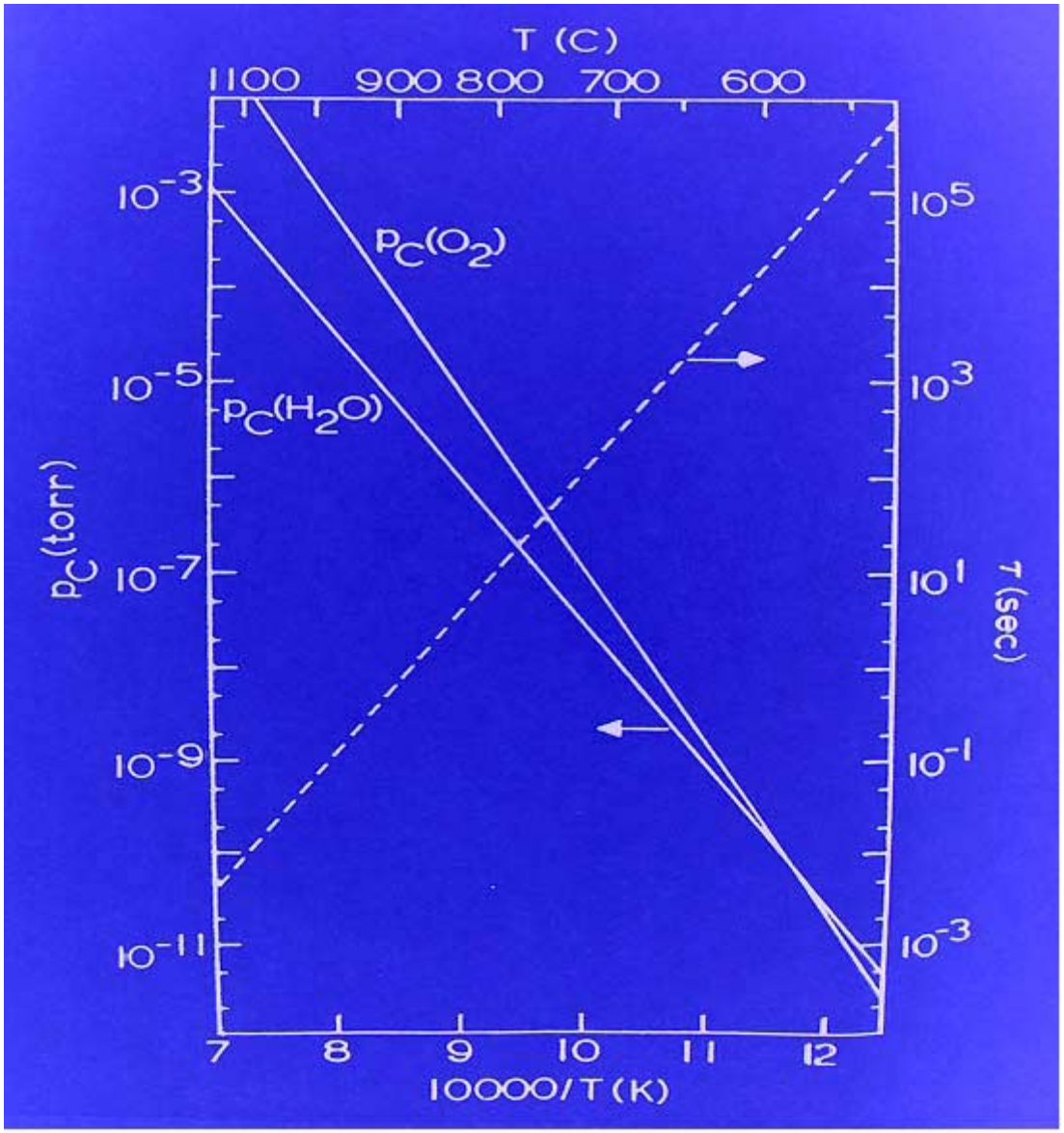
Control

- **Surface-reaction limited**
  - Temperature sensitive
  - Depends on gases and chemical reaction
- **Mass-transport limited**
  - Gas-phase diffusion
  - Sensitive to gas flow
  - Difficult if wafers closely spaced
- ***In-situ* monitoring**
  - Wafer surface temperature
  - Thickness
  - Index of refraction
- **Gas depletion**
- **Uniformity of heating**

Oxygen Control in $Si_{1-x}Ge_x$

- **$Si_{1-x}Ge_x$ has a Very High Affinity for O**
  - At 700C, Growth of Si with 500ppb of H_2O in H_2 Carrier: $O < 10^{17}cm^{-3}$
  - At 700C, Growth of $Si_{0.8}Ge_{0.2}$ with 500ppb of H_2O in H_2 Carrier: $O > 10^{20}cm^{-3}$
- **Methods of O Control**
  - Process at Hard Vacuum
    - UHV/CVD or MBE
  - Process at RP or AP (20torr - 760torr) with Purified Gases
    - Require < ~50ppb O and H_2O in Process Gases
    - H_2
      - Palladium Alloy Diffuser
    - H_2, N_2, SiH_4, GeH_4, HCl
      - Active Cartridge Purifiers
        - Nanochem (Matheson)
        - ATMI
        - Millipore
        - SAES
        - Aeronex

Partial pressure for oxygen incorporation from H_2O and O_2



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Gases for Silicon Epitaxy

	Silane (SiH_4)	Dichlorosilane (SiH_2Cl_2)	Silicon Tetrachloride ($SiCl_4$)
Temperature	1000-1050°C	1050-1100°C	1150-1200°C
Reaction	$SiH_4 \rightarrow Si + 2H_2$	$SiH_2Cl_2 \rightarrow Si + 2HCl$	$SiCl_4 + 2H_2 \rightarrow Si + 4HCl$
Reversible	No	Yes	Yes
HCl Byproduct	No	Yes	Yes
Gas-Phase Nucleation	Yes	No	No
Deposition Rate	0.2 µm/min	~1 µm/min	>2 µm/min
Flow Control	Easy	Moderate	Difficult
Cost	High	Moderate	Low
Danger	High	Moderate	Moderate
Used for	Thinner Layers	Many Layers	Thicker Layers

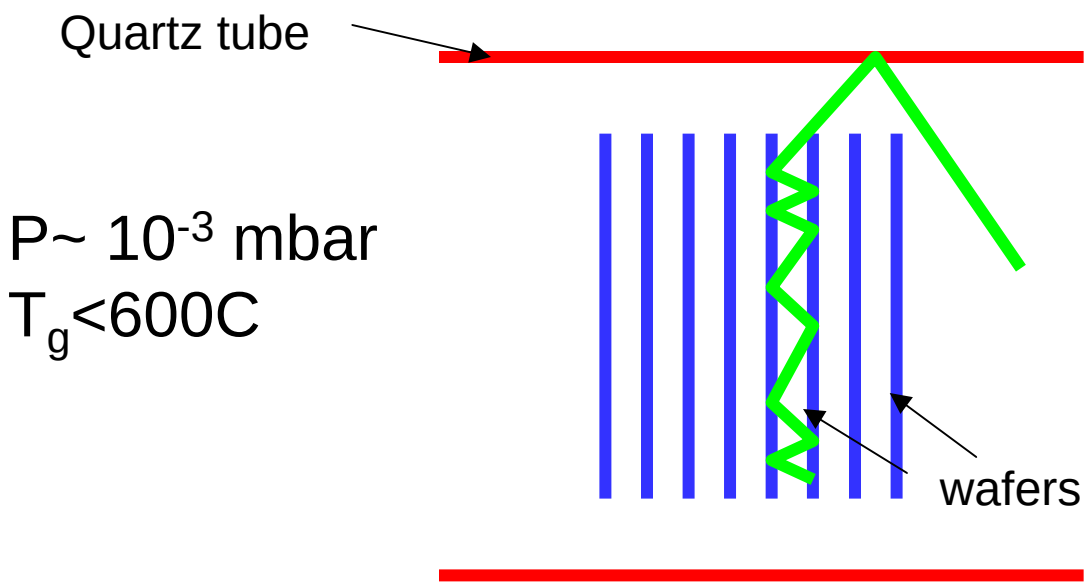
AIXTRON's flexible epi systems for Strained Si / SiGe

Tricent® vs. Multiwafer Reactor®

Tricent SiGe Cluster Tool: 150, 200 or 300 mm

AIX 2600G3: up to 7x150 or 3x200 mm

SiGe UHVCVD

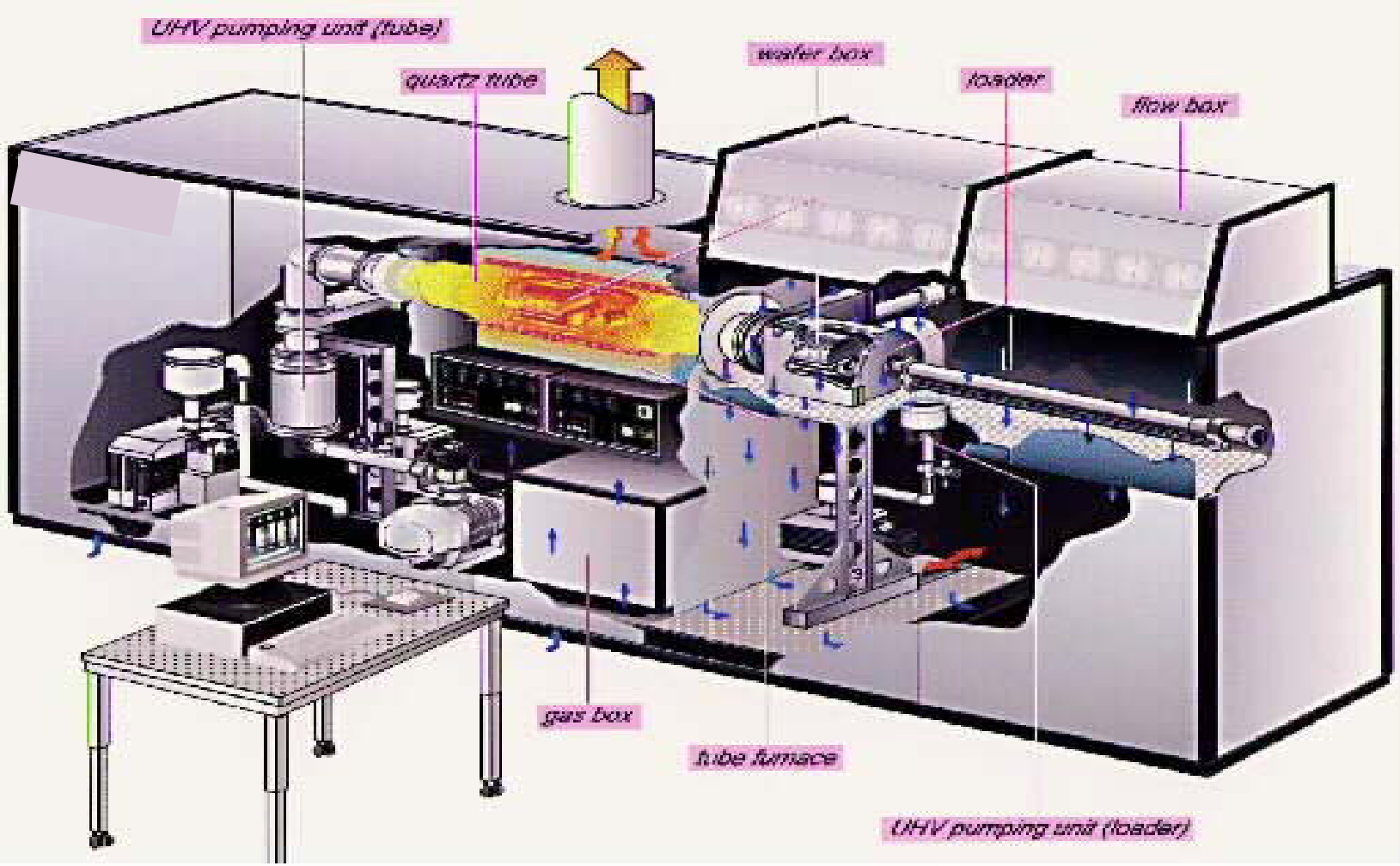


P~ 10^{-3} mbar
T_g<600C

SiH_4
GeH_4
B_2H_6
PH_3

molecular flow Ā uniform growth
sticking coefficients~10^{-3}
UHV initial conditions, P~10^{-9} m bar
hydrogen terminated Si wafers at start

Hot wall UHVCVD Batch tool



Product Information

EPIGRESS UH254/256/258
UHV-CVD SYSTEM FOR SiGe

THE TECHNIQUE OF CHOICE

UHV-CVD is the technique of choice for large-scale deposition of SiGe. The process is operated under surface-kinetics limited conditions, which Epigress UHV-CVD system takes full advantage of. Homogeneous growth is obtained on up to 25 of 4 to 8-inch wafers.

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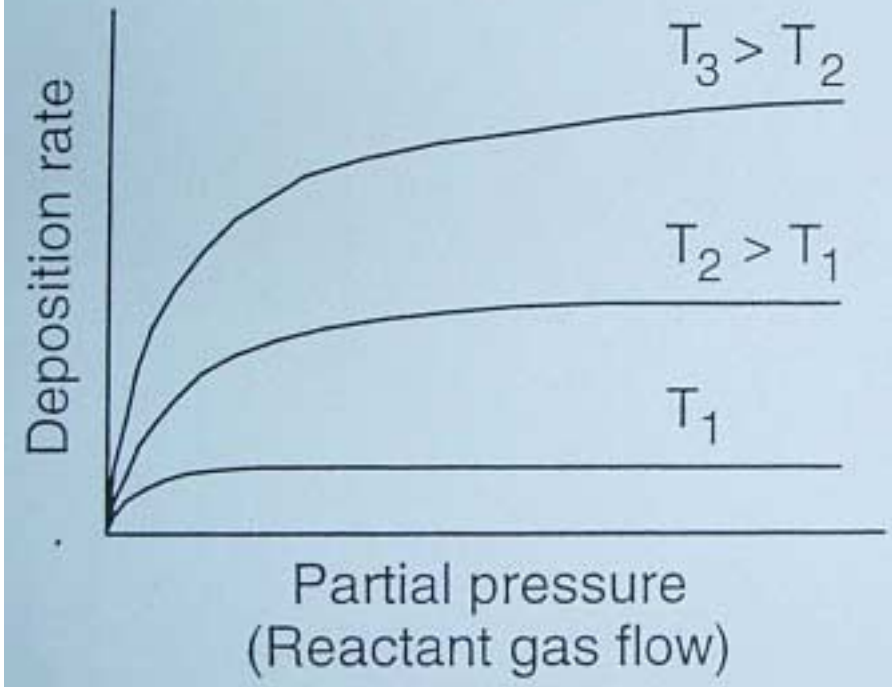
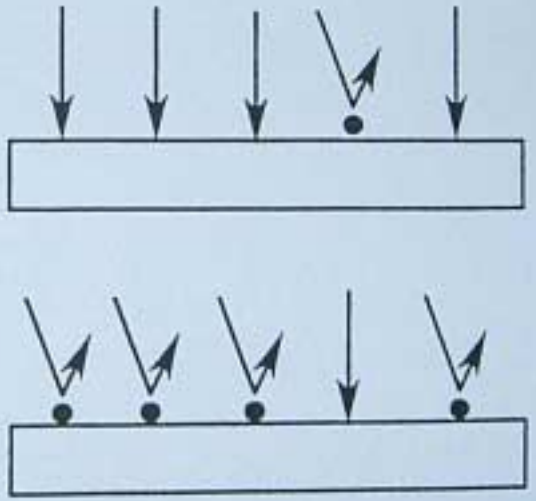
Single-Wafer Reactors

Economics require high deposition rate

- Higher temperature
- Higher reactant-gas partial pressure



Limited by adsorbed layer



$$R_D = \frac{A\, P_{SiH_4}}{1 + B\, P_{SiH_4}}$$

Can use more reactive gas
eg, Si_2H_6, instead of SiH_4

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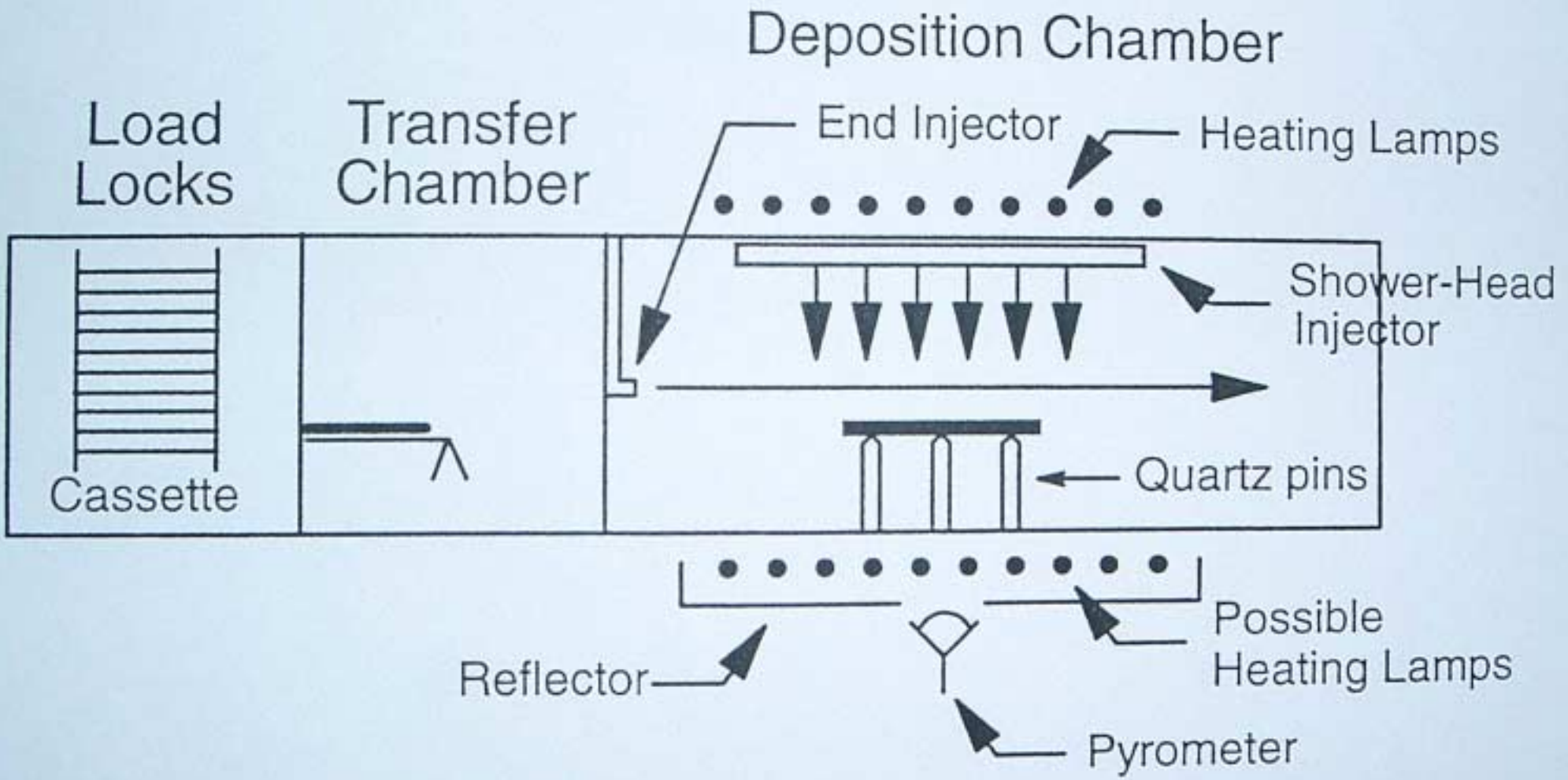
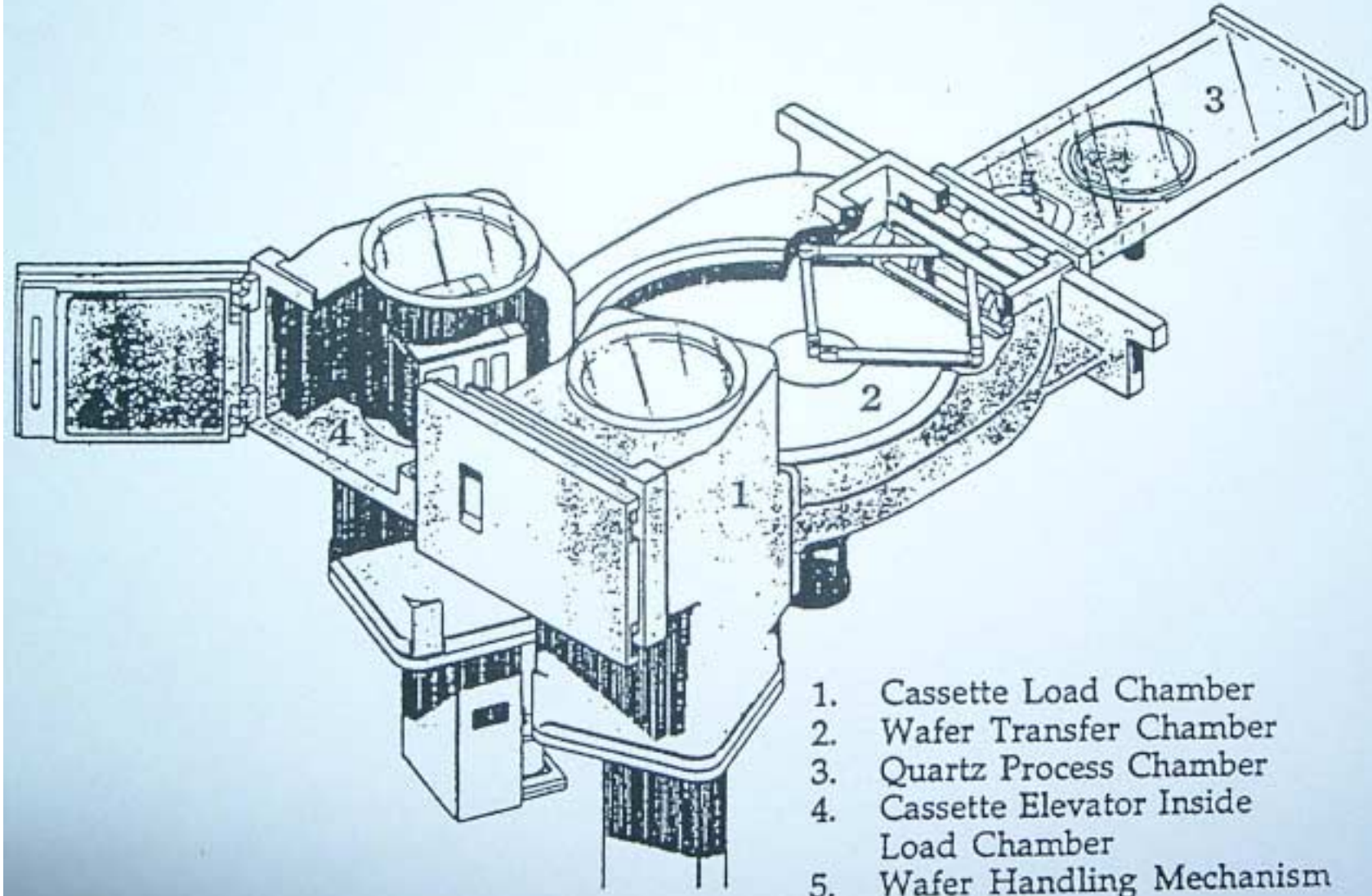
Single-Wafer Reactor (Low-Thermal Mass)



SINGLE–WAFER REACTOR WITH LOAD LOCK AND SUPPORT PLATE



1. Cassette Load Chamber
2. Wafer Transfer Chamber
3. Quartz Process Chamber
4. Cassette Elevator Inside Load Chamber
5. Wafer Handling Mechanism

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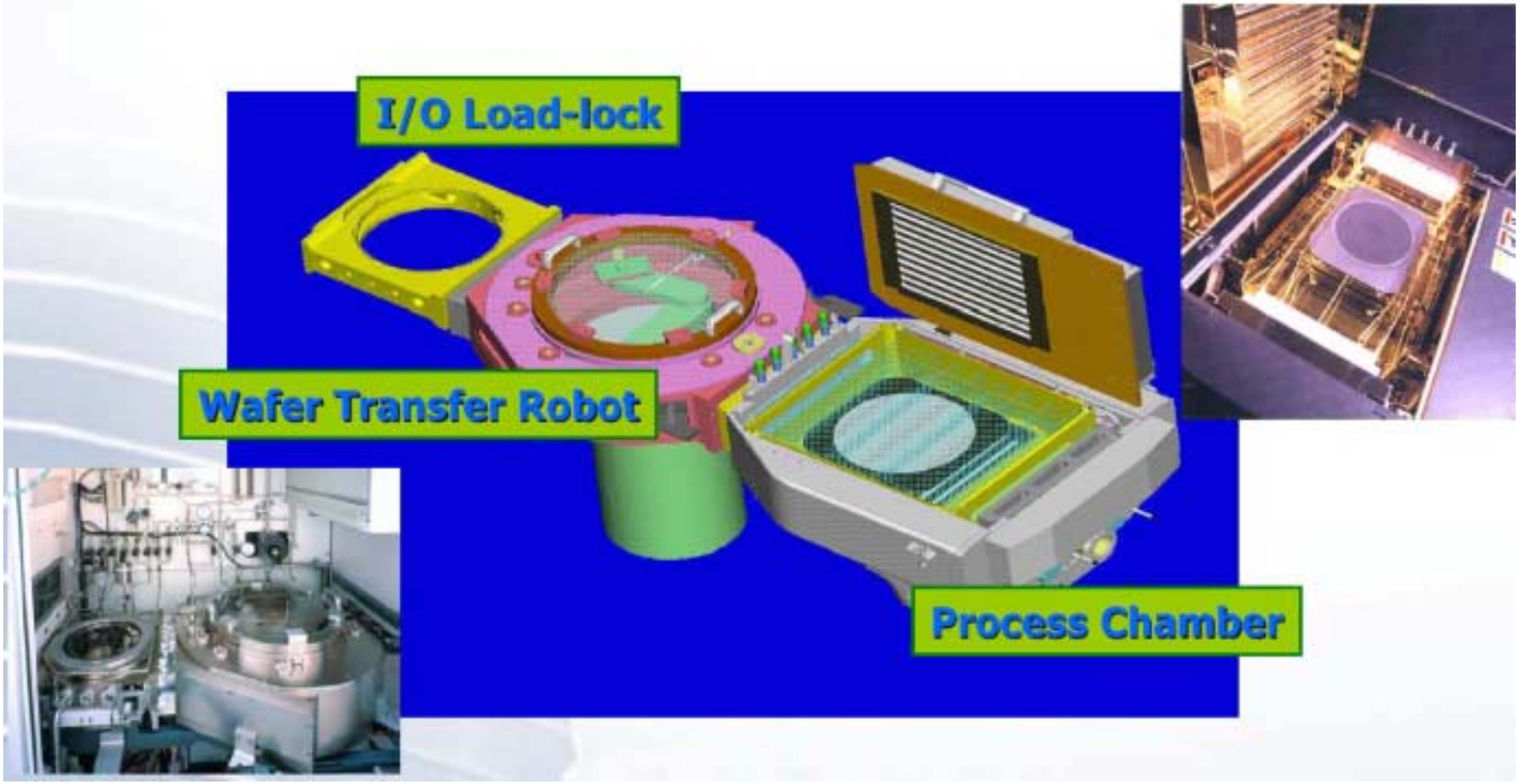
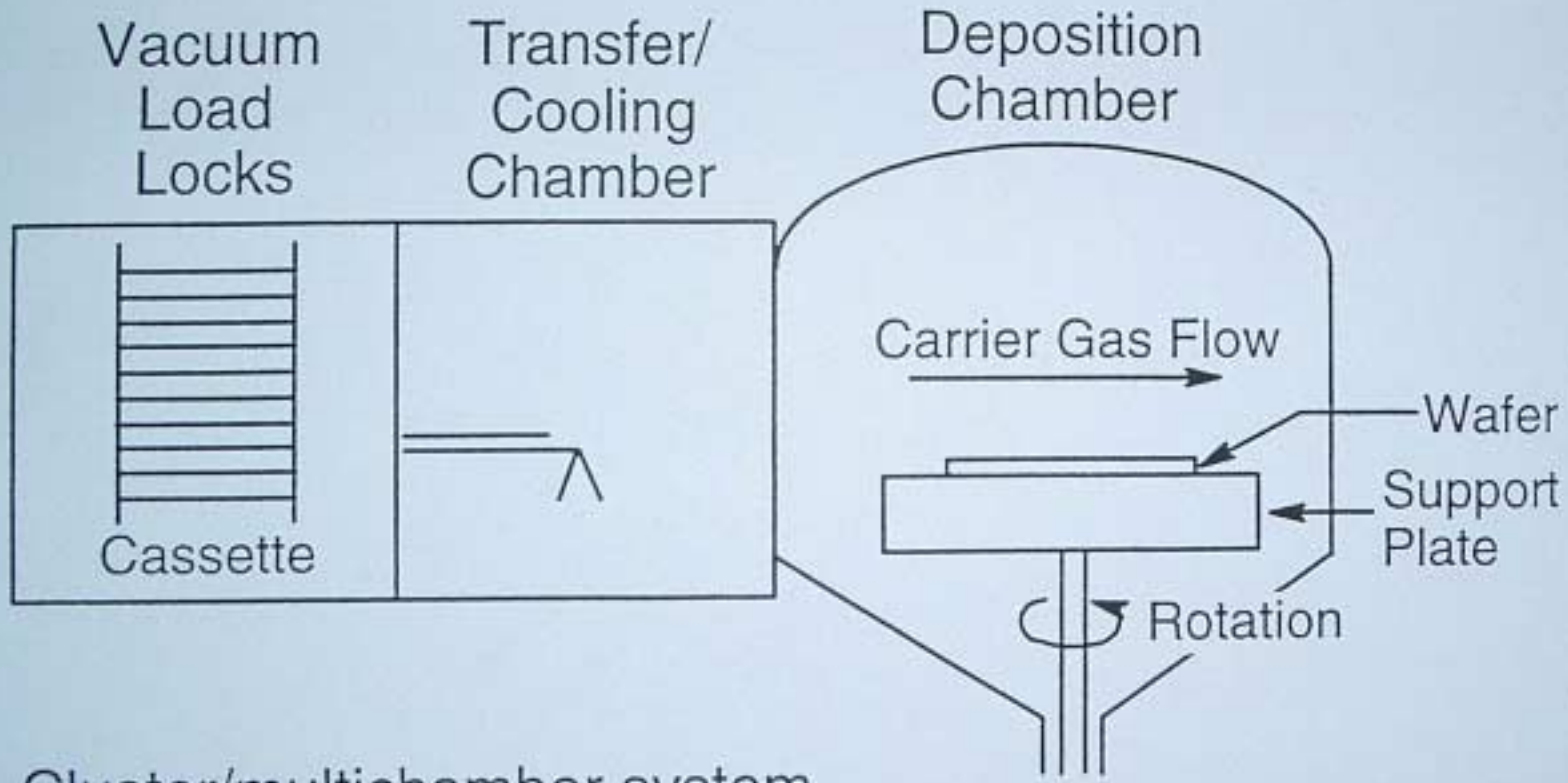
Configuration of ASM's Epsilon 3000



Applied Materials Centura



Cluster/multichamber system

RP wafer transfer

Cooldown chamber

Chamber volume: 11 liters

P ~ 1 - 600 Torr

T ~ 550 - 1200°C

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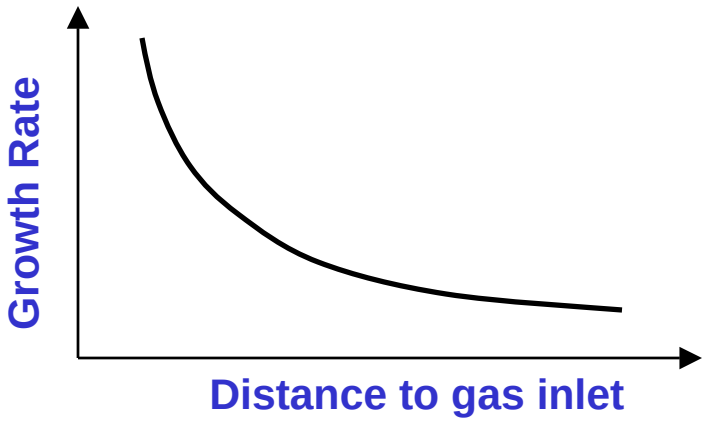
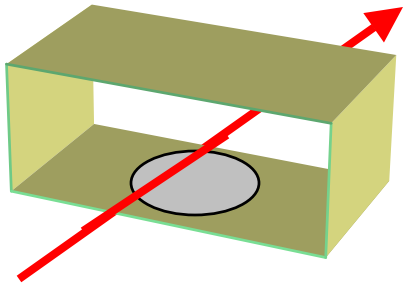
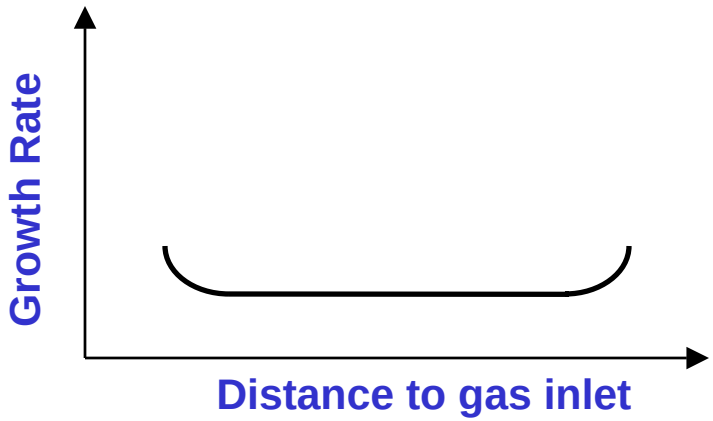
Uniform Gas Distribution by AIXTRON´s Closed Coupled Showerhead

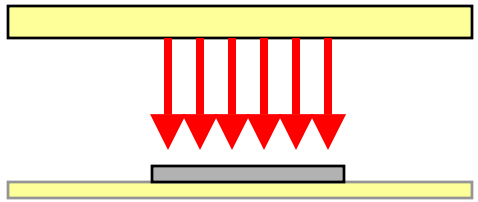
Horizontal Quarz Tube Reactor





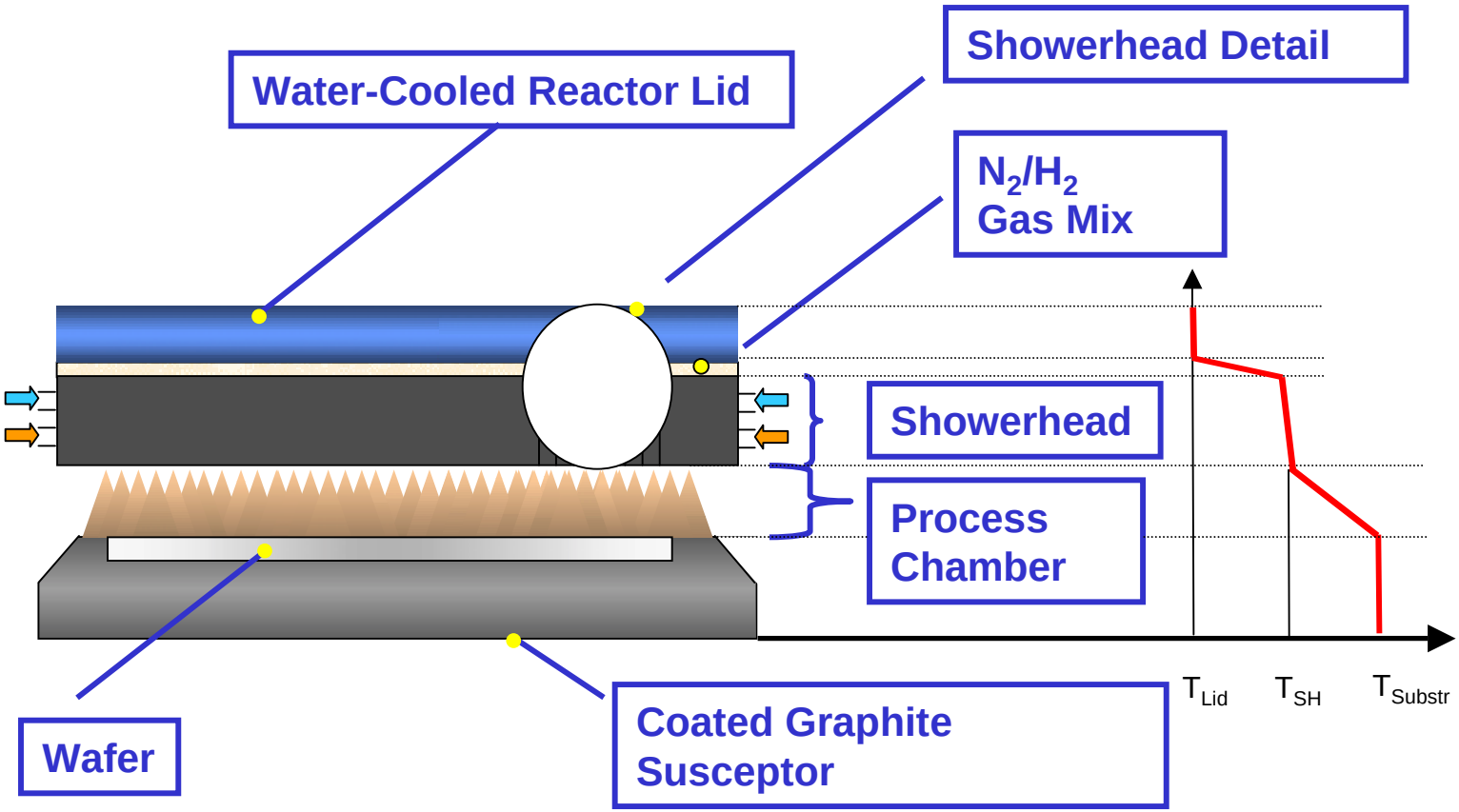
Closed Coupled Showerhead Reactor





SiGe Tricent®

Dual-Chamber Showerhead (pat. pend.)

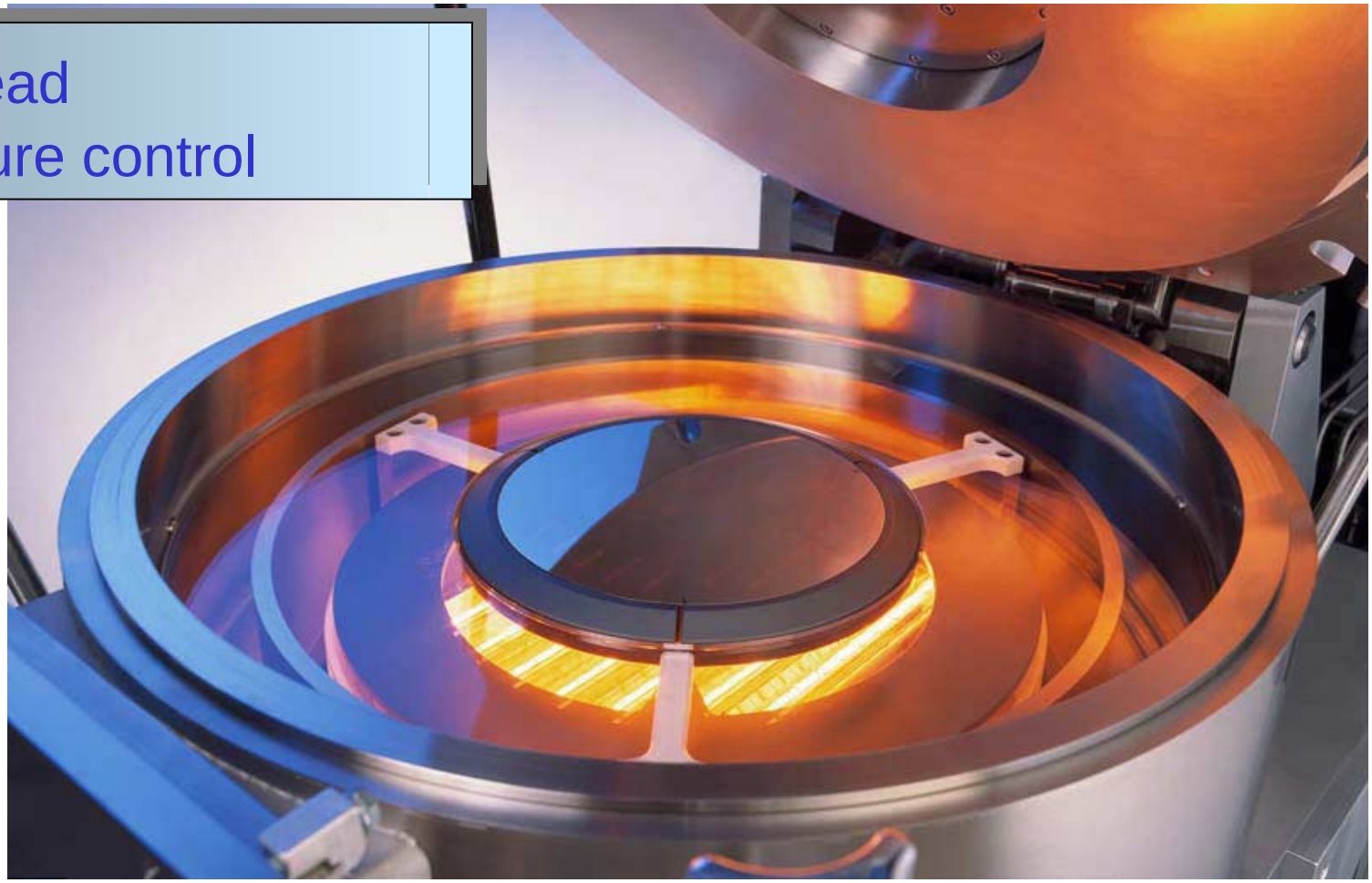


Temperature Control Concept

SiGe Tricent®

Unique CVD chamber features developed beyond industry standards

- Showerhead
- Temperature control



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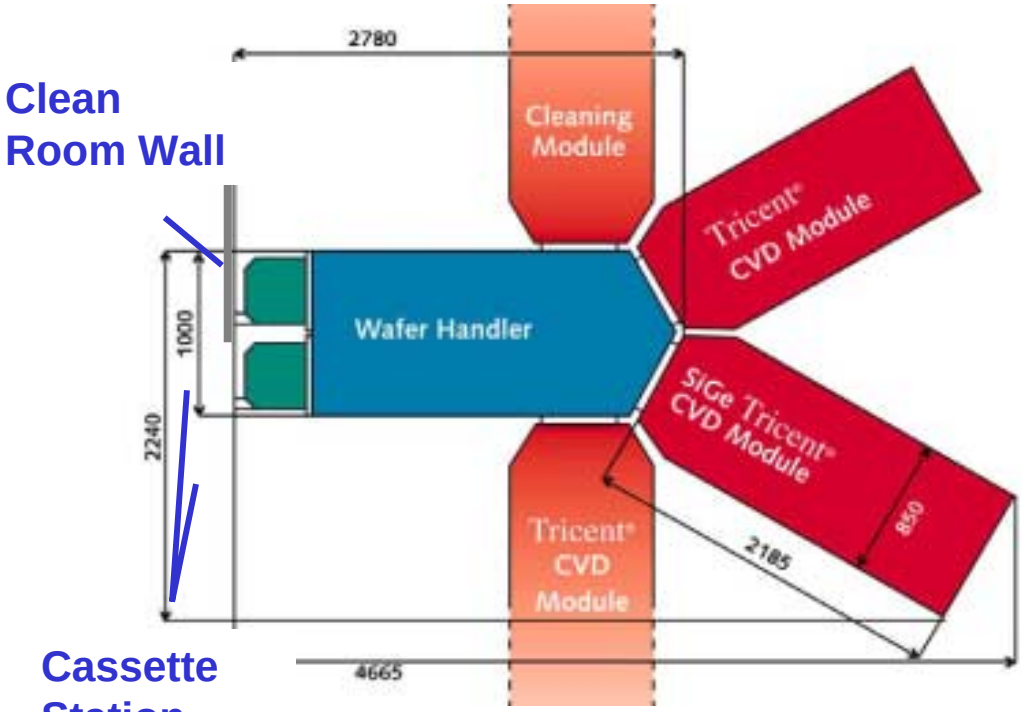
Tricent®

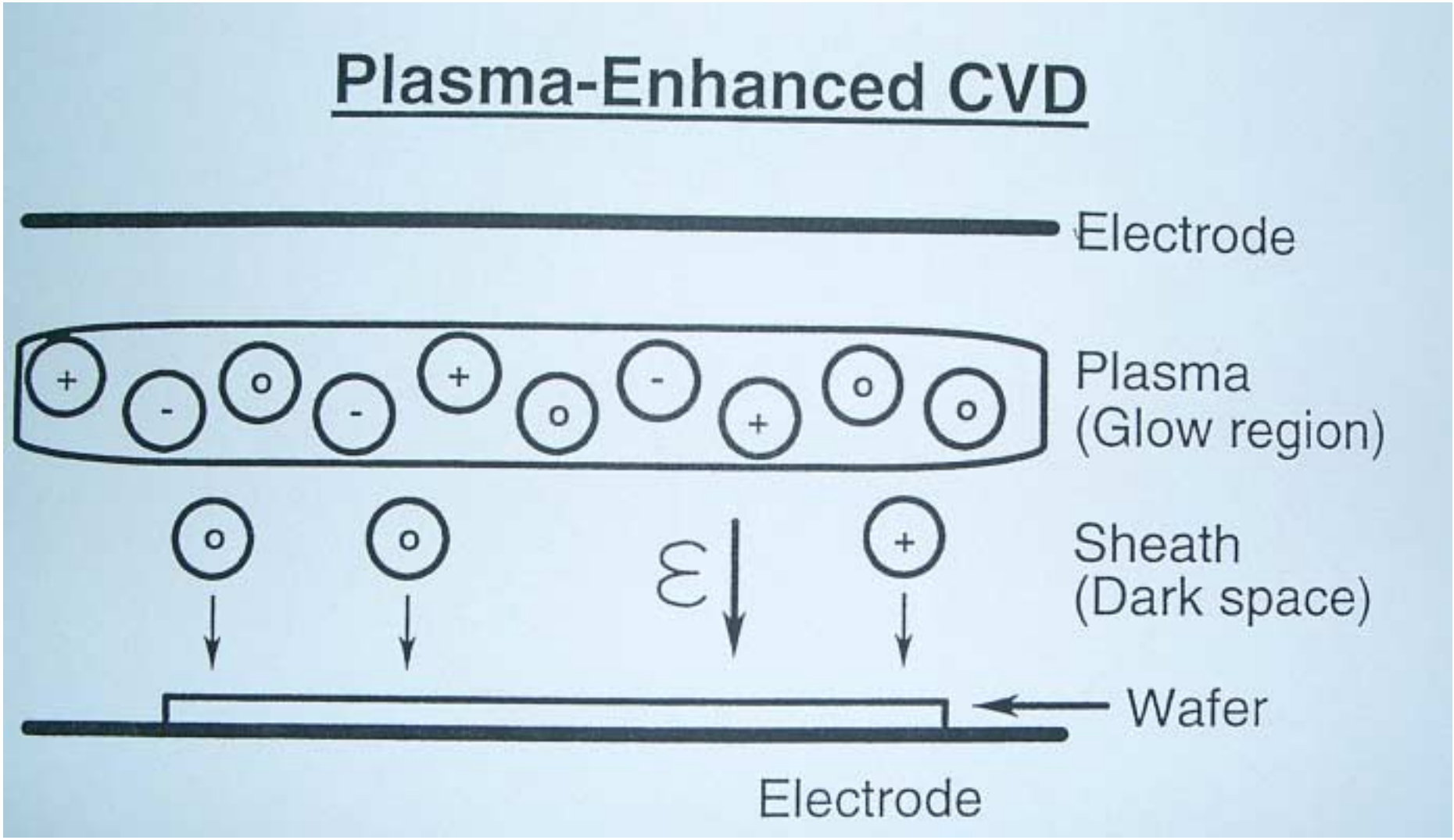
Customer Process Support



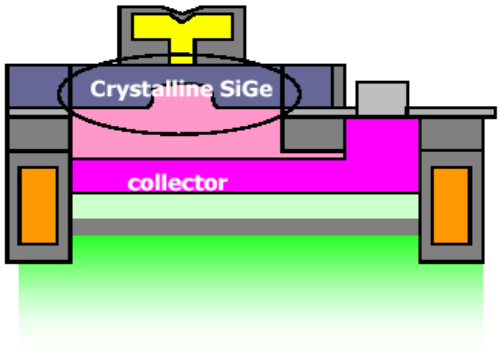
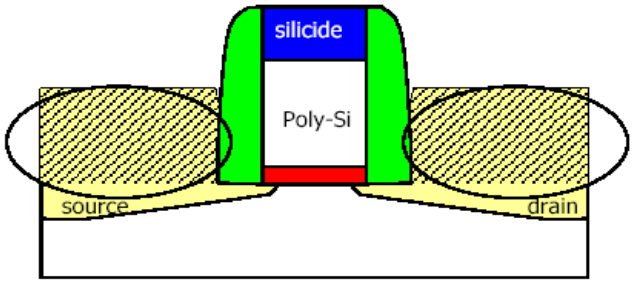
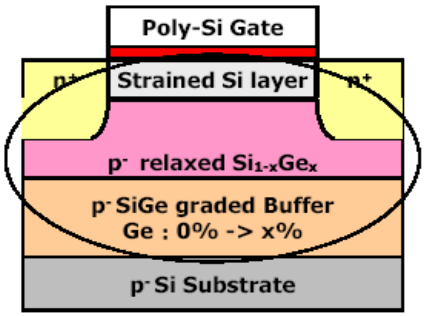
Process platform for
HBTs, HFETs and BiCMOS
- pure Silicon Growth
- differential SiGe:C growth
- selective SiGe:C growth
- SiGe on SOI

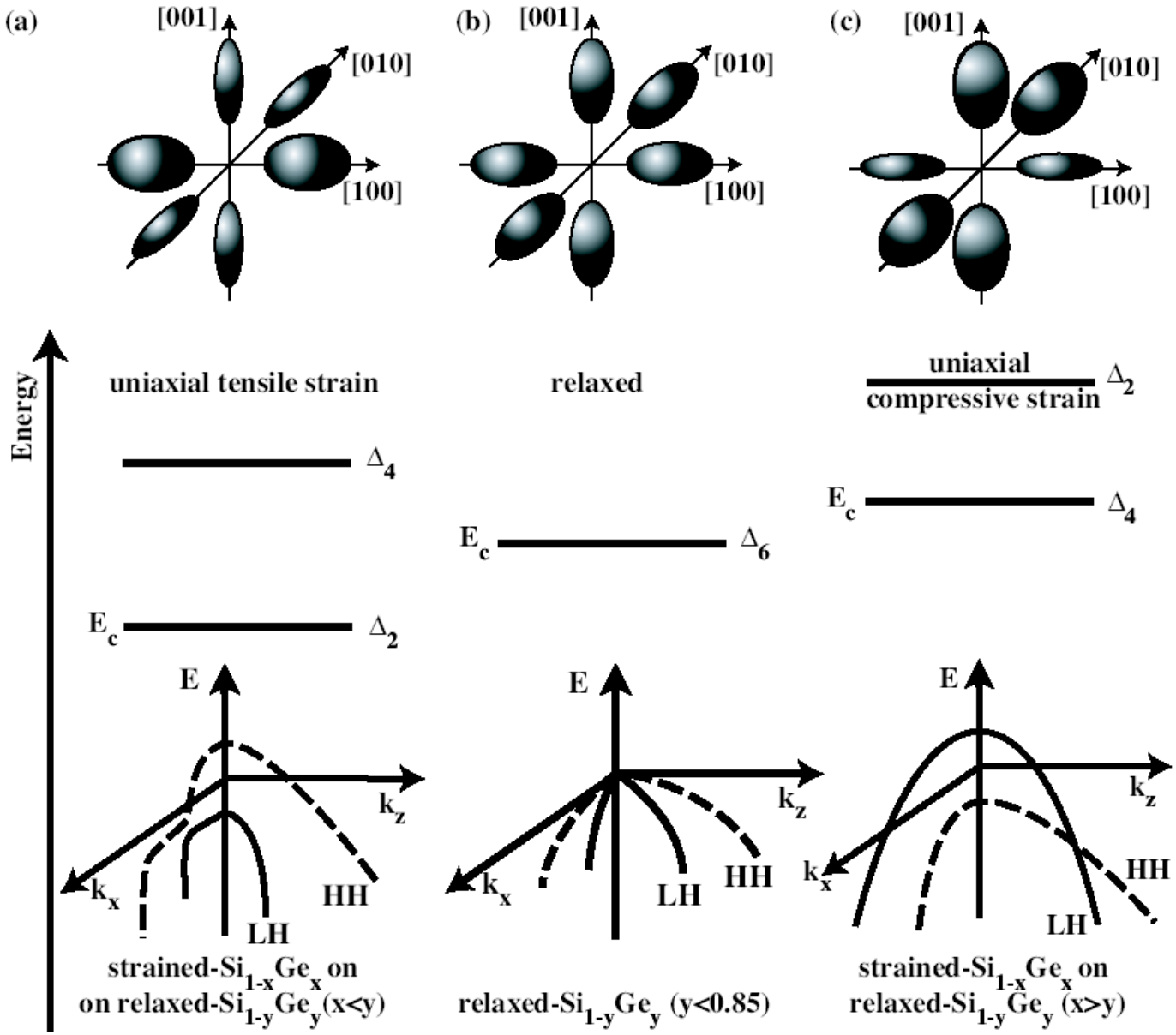
Temp		Process Gas Sources
550-680°C	SiGe:C	SiH4 + GeH4 + SiCH6
650-750°C	SiGe	SiH4 + GeH4
730-800°C	sel. SiGe	SiH2Cl2 + HCl + GeH4
800-900°C	SEG	SiH2Cl2 + HCl

Plasma-Enhanced CVD

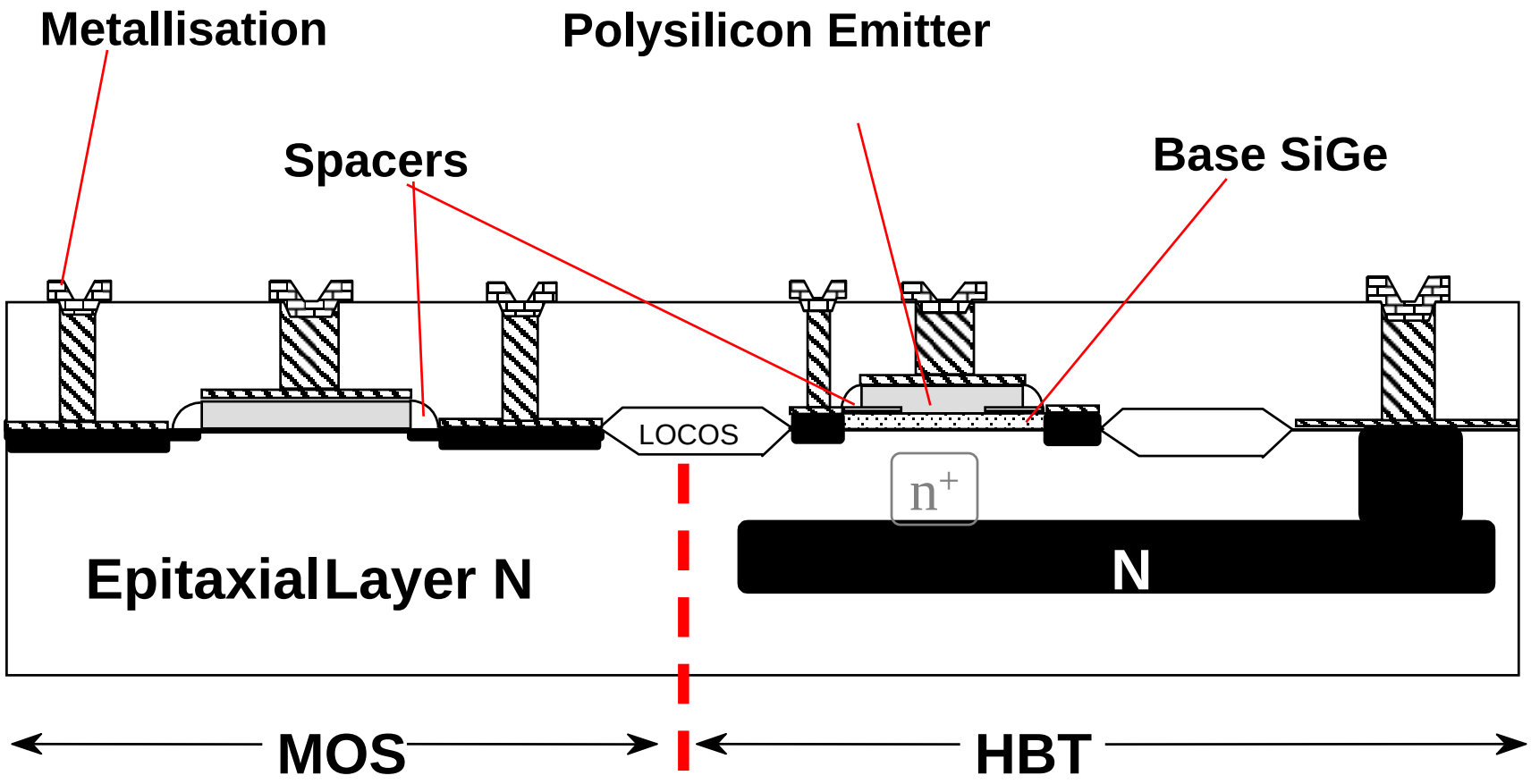


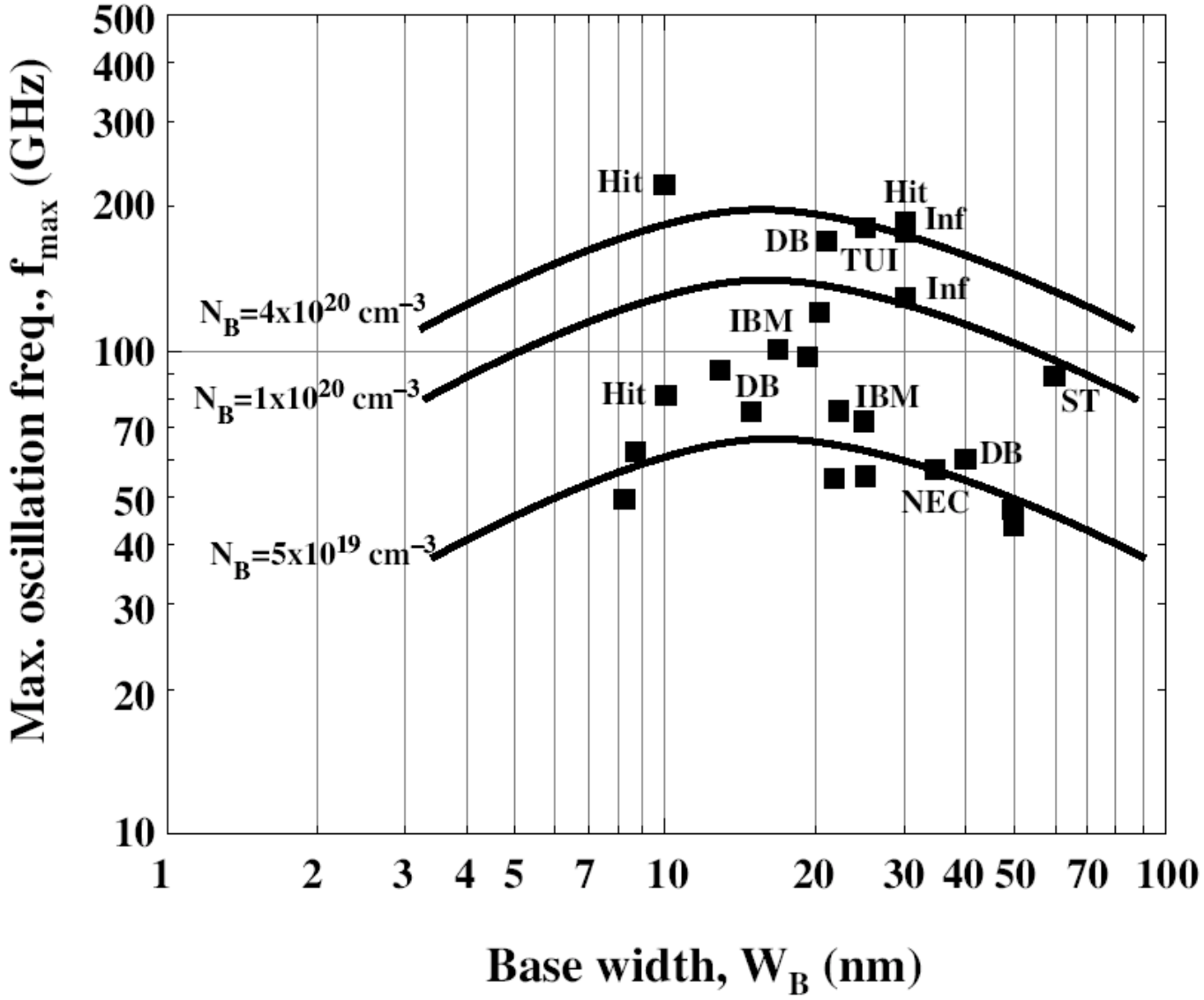
SiGe Epitaxy Application

	SiGe base HBT	MOSFET	
Device Structure			
Location of use	Bipolar transistor Base Layer	Elevated Source Drain	Strained Channel
Key Issue	High frequency (F_t, F_{max})	Ultra Shallow Junction	Carrier mobility in channel
Key Process Parameter	Crystallinity Dopant & Ge fraction Control Productivity	Selectivity Productivity	Productivity

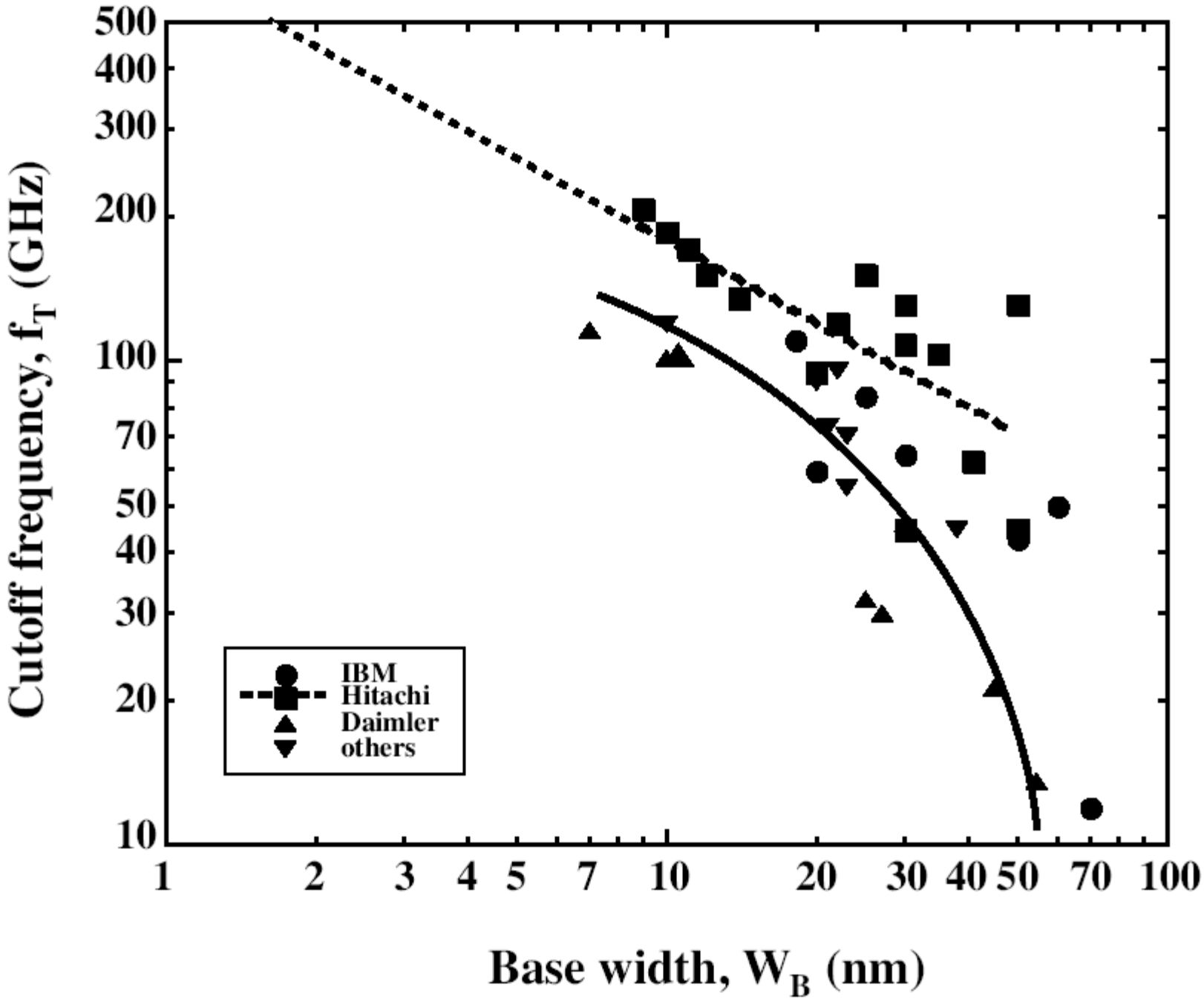

(a)
[001]
[010]
[100]
(b)
[001]
[010]
[100]
(c)
[001]
[010]
[100]
Energy
uniaxial tensile strain
relaxed
uniaxial
compressive strain
Δ_2
Δ_4
E_c
Δ_4
E_c
Δ_6
E_c
Δ_2
E
k_z
k_x
HH
LH
strained-$Si_{1-x}Ge_x$ on
on relaxed-$Si_{1-y}Ge_y$(x<y)
relaxed-$Si_{1-y}Ge_y$ (y<0.85)
strained-$Si_{1-x}Ge_x$ on
relaxed-$Si_{1-y}Ge_y$ (x>y)

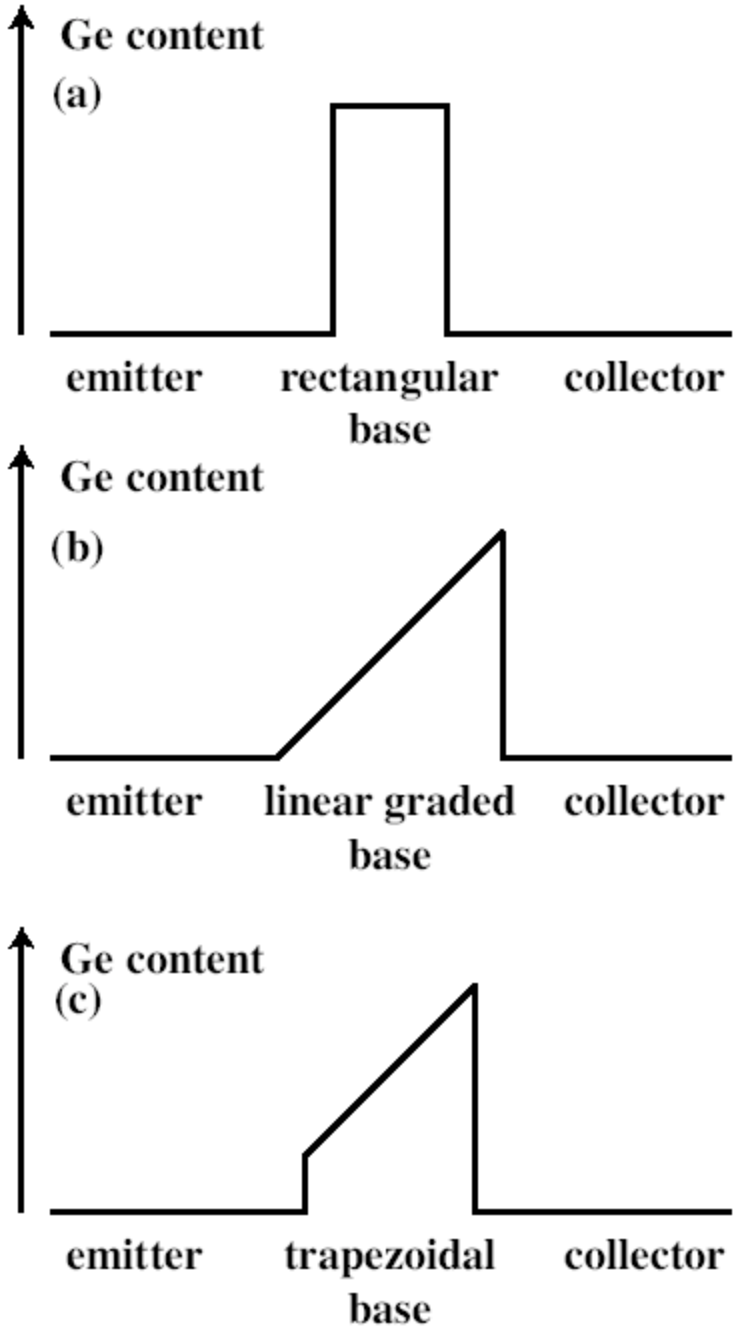
SiGe HBT in a BiCMOS flow



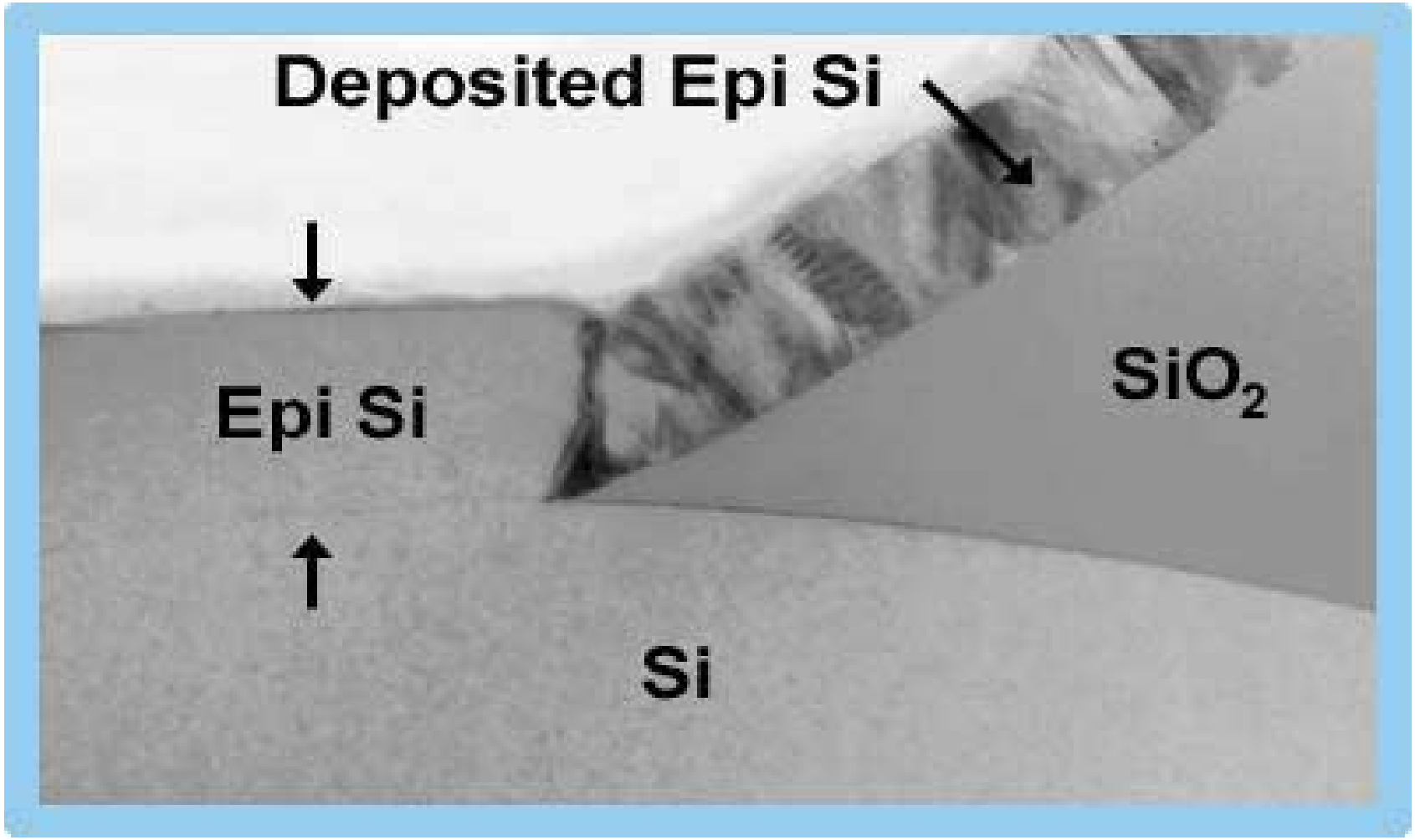

Max. oscillation freq., f_{max} (GHz)
500
400
300
200
100
70
50
40
30
20
10
1
2
3
4
5
7
10
20
30
40
50
70
100
Base width, W_B (nm)
N_B=4x10^{20} cm^{-3}
N_B=1x10^{20} cm^{-3}
N_B=5x10^{19} cm^{-3}
Hit
Hit
Inf
DB
TUI
Inf
IBM
Hit
DB
IBM
ST
DB
NEC

AIXTRON

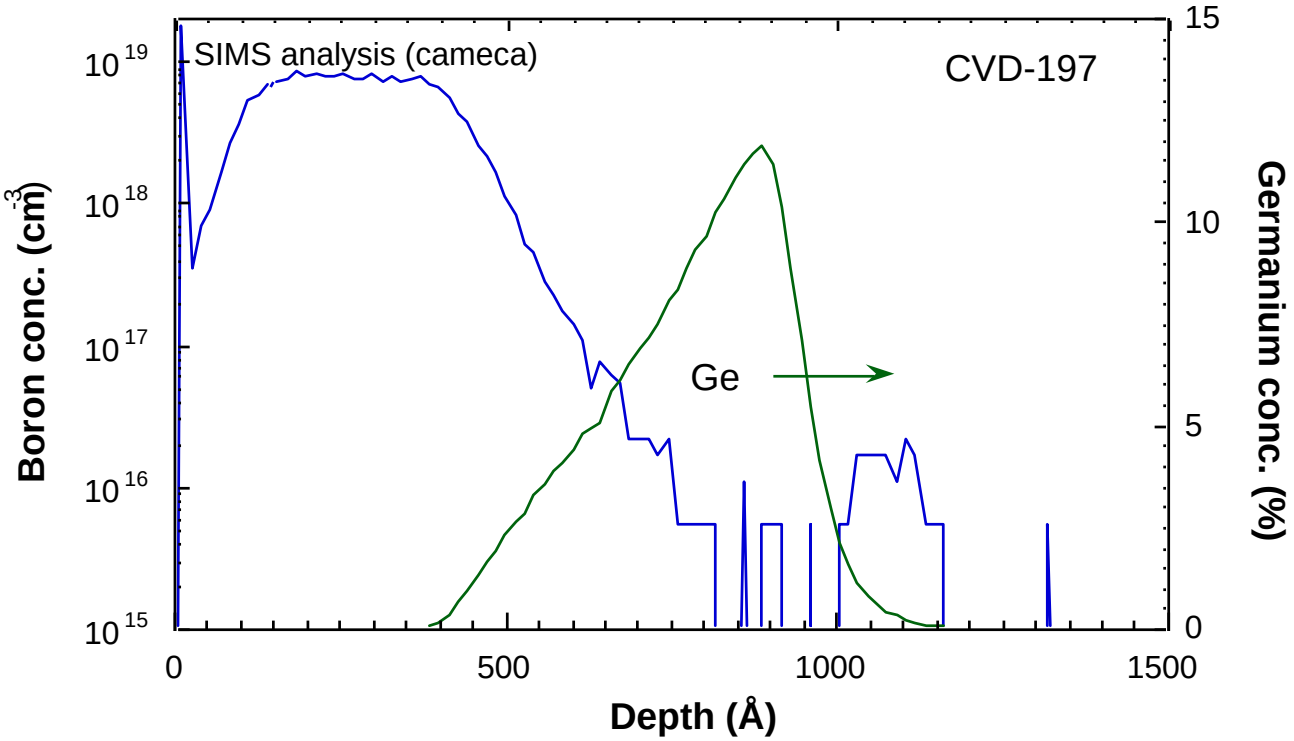

Cutoff frequency, f_T (GHz)
500
400
300
200
100
70
50
40
30
20
10
1
2
3
4
5
7
10
20
30
40
50
70
100
Base width, W_B (nm)
IBM
Hitachi
Daimler
others


Ge content
(a)
emitter
rectangular base
collector
Ge content
(b)
emitter
linear graded base
collector
Ge content
(c)
emitter
trapezoidal base
collector

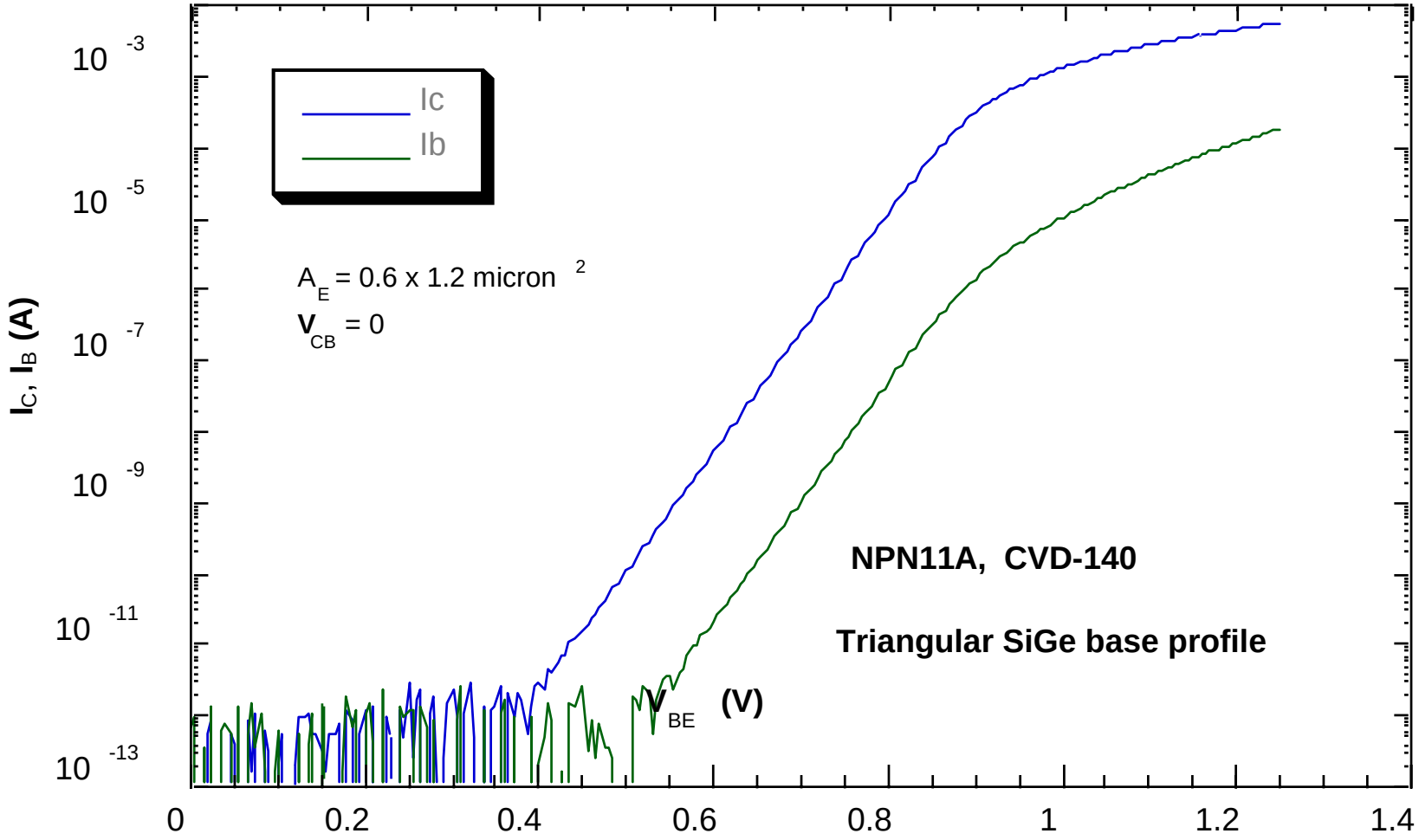
XTEM of Si deposition on Si/oxide



HBT base structure SIMS profiling



Gummel Plot, npn HBT



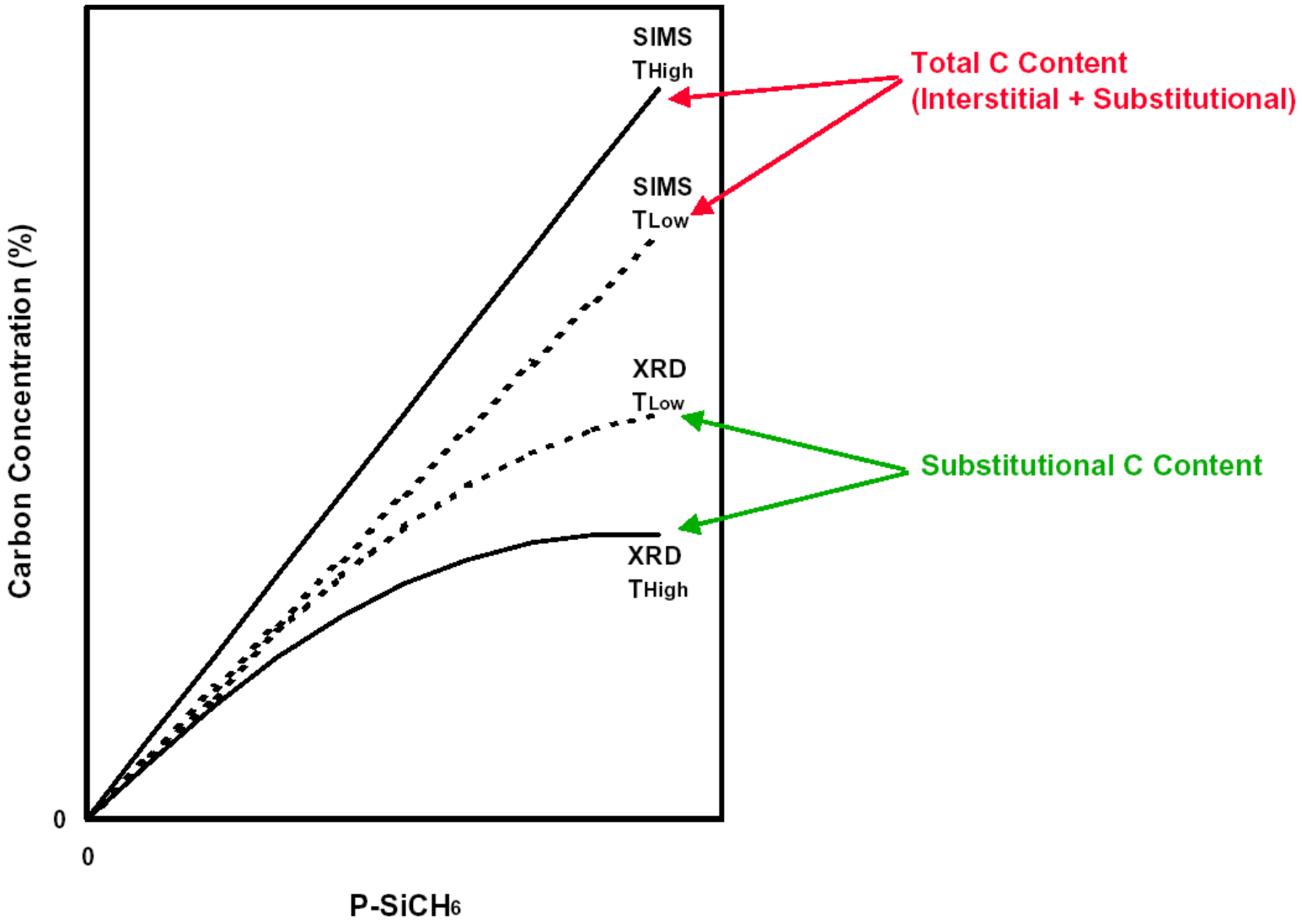
$Si_{1-x}Ge_x$:C

- **Why Add C to $Si_{1-x}Ge_x$?**
  - Adding 0.5% to 1% C Greatly Reduces B Diffusion
    - $D_{B, Si} > D_{B, SiGe} > D_{B,SiGe:C}$
  - Compensate Strain in $Si_{1-x}Ge_x$ for Improved Thermal Stability
    - Add Approx. 1 atom of C per 9 atoms of Ge

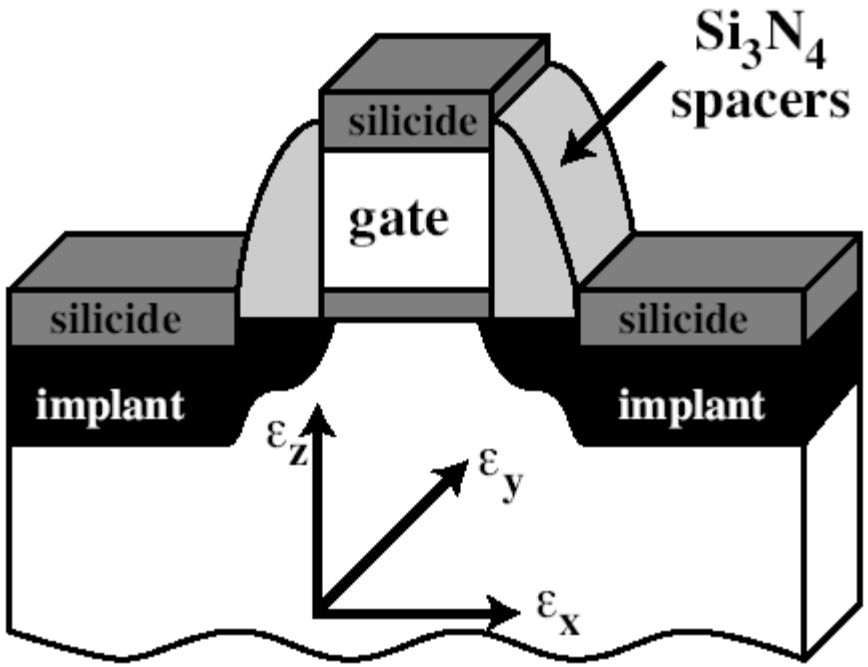
- **Issues Regarding C Addition to $Si_{1-x}Ge_x$**
  - C ***Must*** be Substitutional in Crystal Lattice to Suppress B Diffusion
    - Deposition Temp. < 625C
    - Higher Deposition Temp. Results in Interstitial C
      - Can Cause Amorphous Film Characteristics for C > ~3%

- **Precursors for C Addition**
  - $SiCH_6$ (Typically 0.1% to 1% $SiCH_6$ in H_2)
  - C_2H_4 (Ethene or Acetylene), C_5H_8 (Cyclopentane)
  - Simple Alkanes, e.g. CH_4, C_2H_6, C_3H_8 etc. Do Not Decompose Adequately

Effect of $Si_{0.8}Ge_{0.2}$ Deposition Temperature on Substitutional vs. Interstitial C Incorporation



CMOS transistor



Advantages:

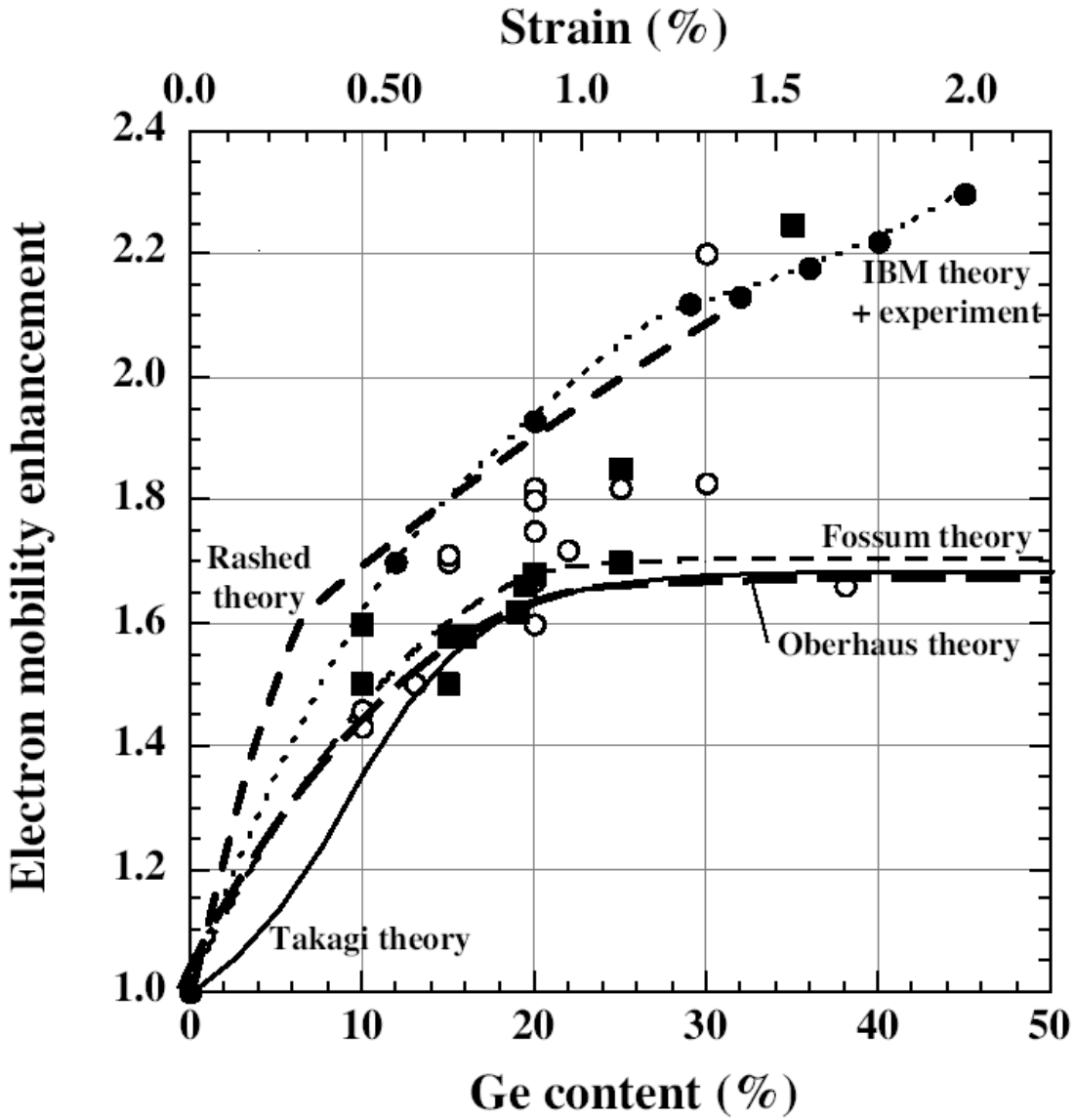
Bulk electron and hole mobility is enhanced in Strained Si:
For p-MOSFET, hole mobility increases for Ge content up to 30-40%, while for n-MOSFET, the electron mobility saturates at about 20% of Ge.

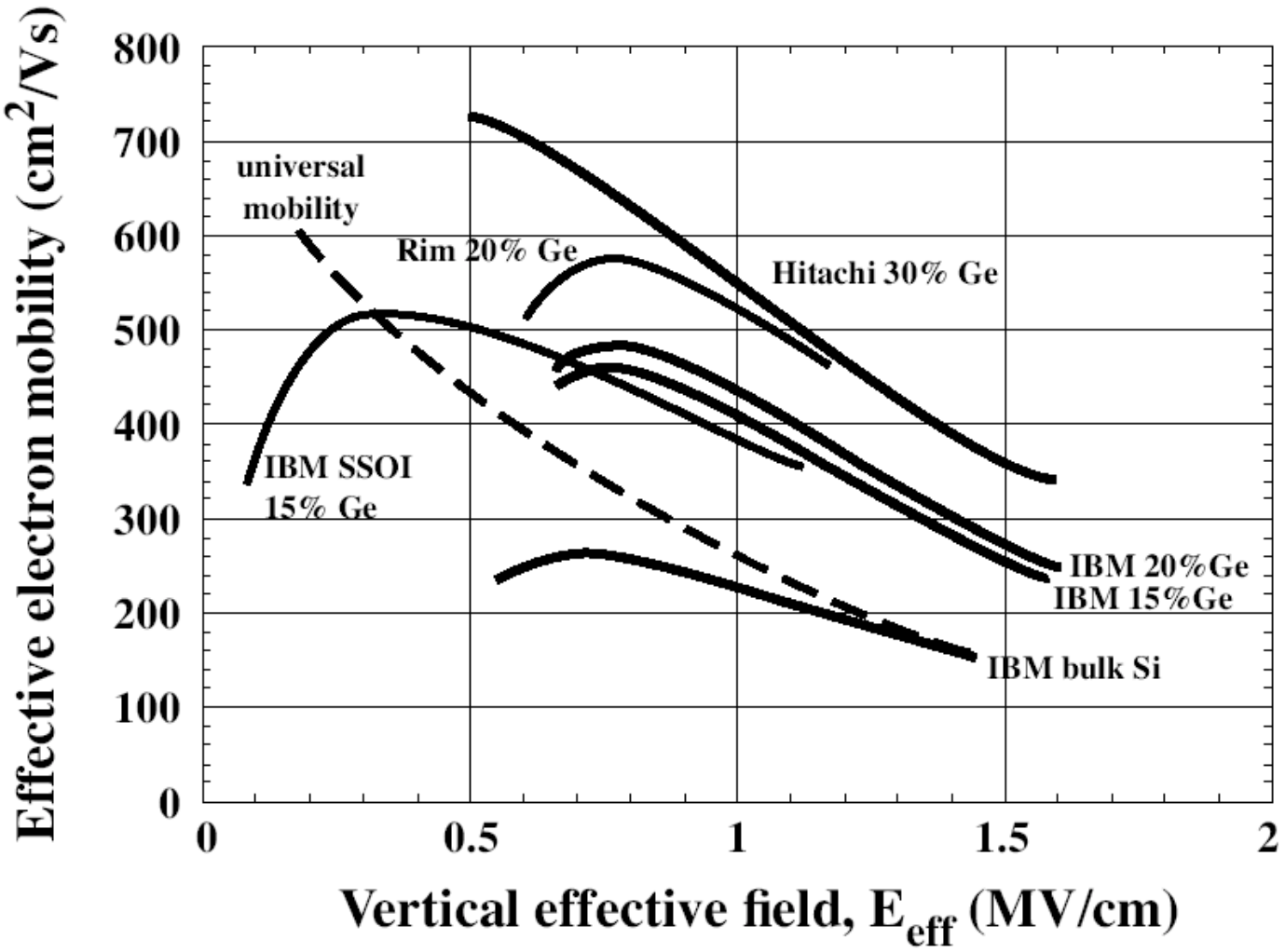
Reported Improvements:

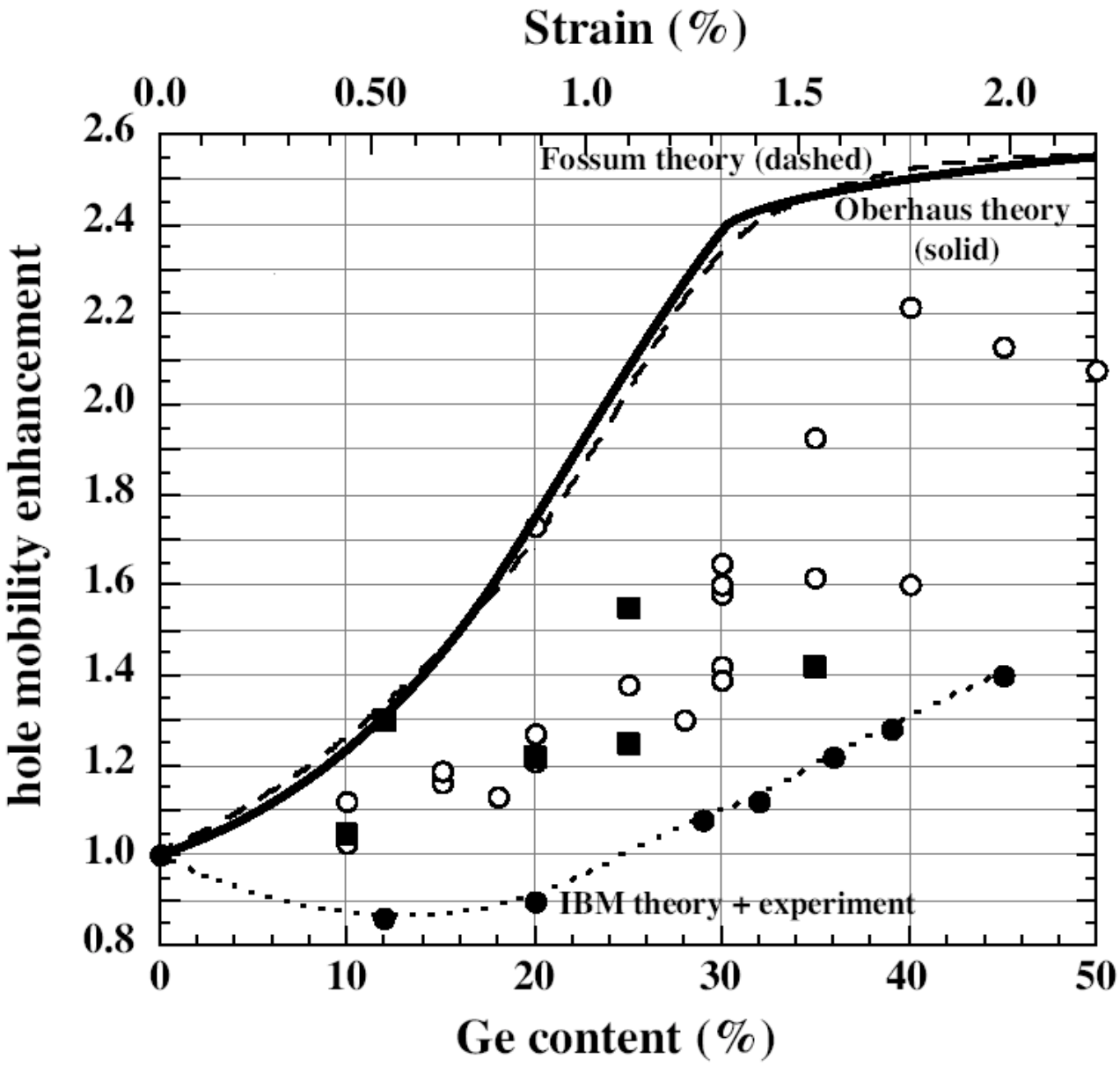
- Electron mobilities > 70 % on bulk Si NMOS is reported by IBM which translates into > 35% Id improvement (VLSI '01)
- Electron mobilities of > 50 % and hole mobilities 15-20 % on SOI is reported by IBM (VLSI '01)
- Electron mobilities of 1.7x on SOI is reported by Hoyt (IEEE El. Dev. Letr '01)
- Electron mobilities > 75 % on bulk Si is reported by Hoyt, Gibbons & Rim (IEEE Trans, '00)

Key issues:

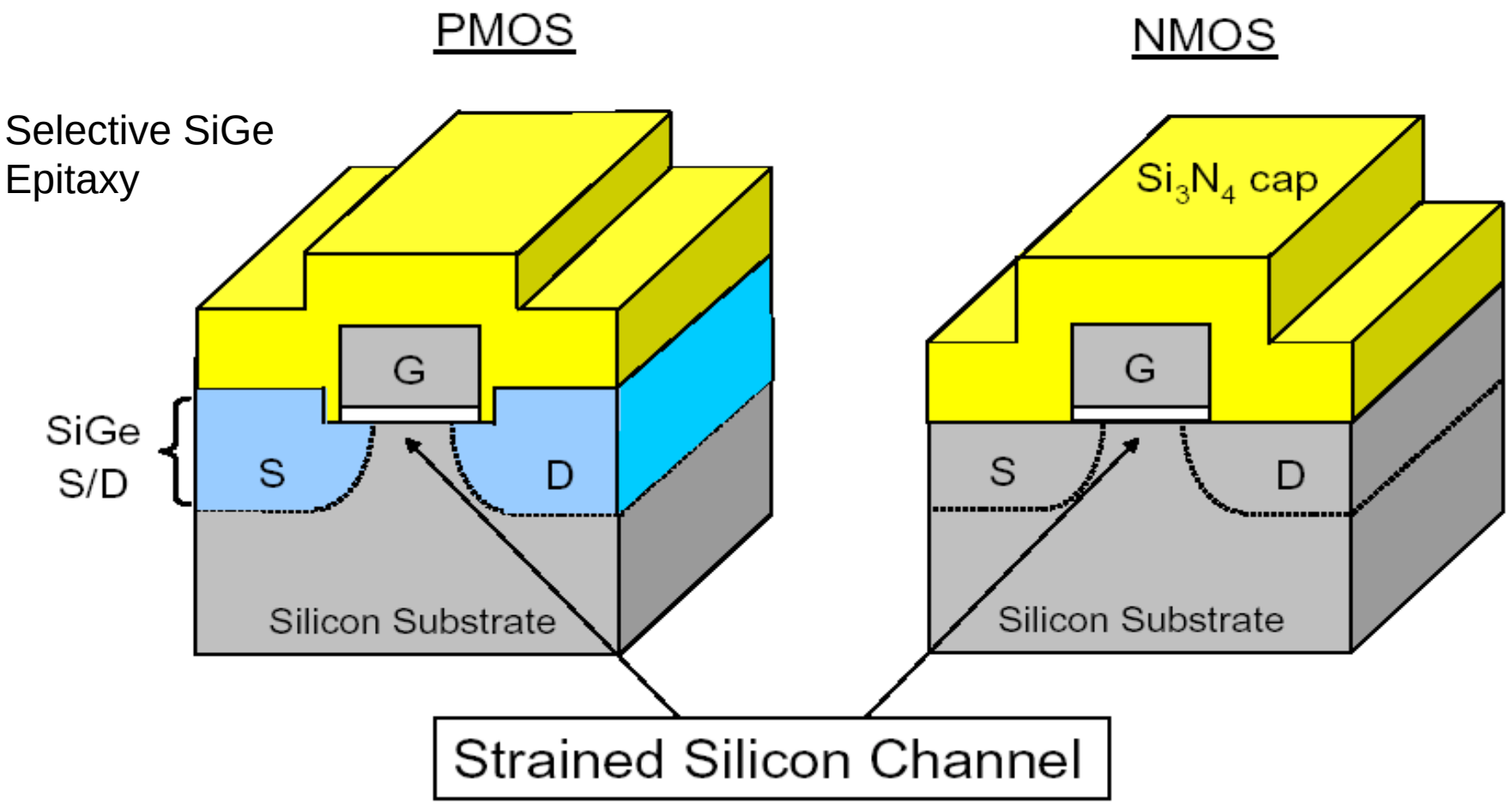
- Gate Oxidation
- Device Isolation
- Self Heating
- Growth rate - cost
- Defect density at surface
- Process integration difficulties

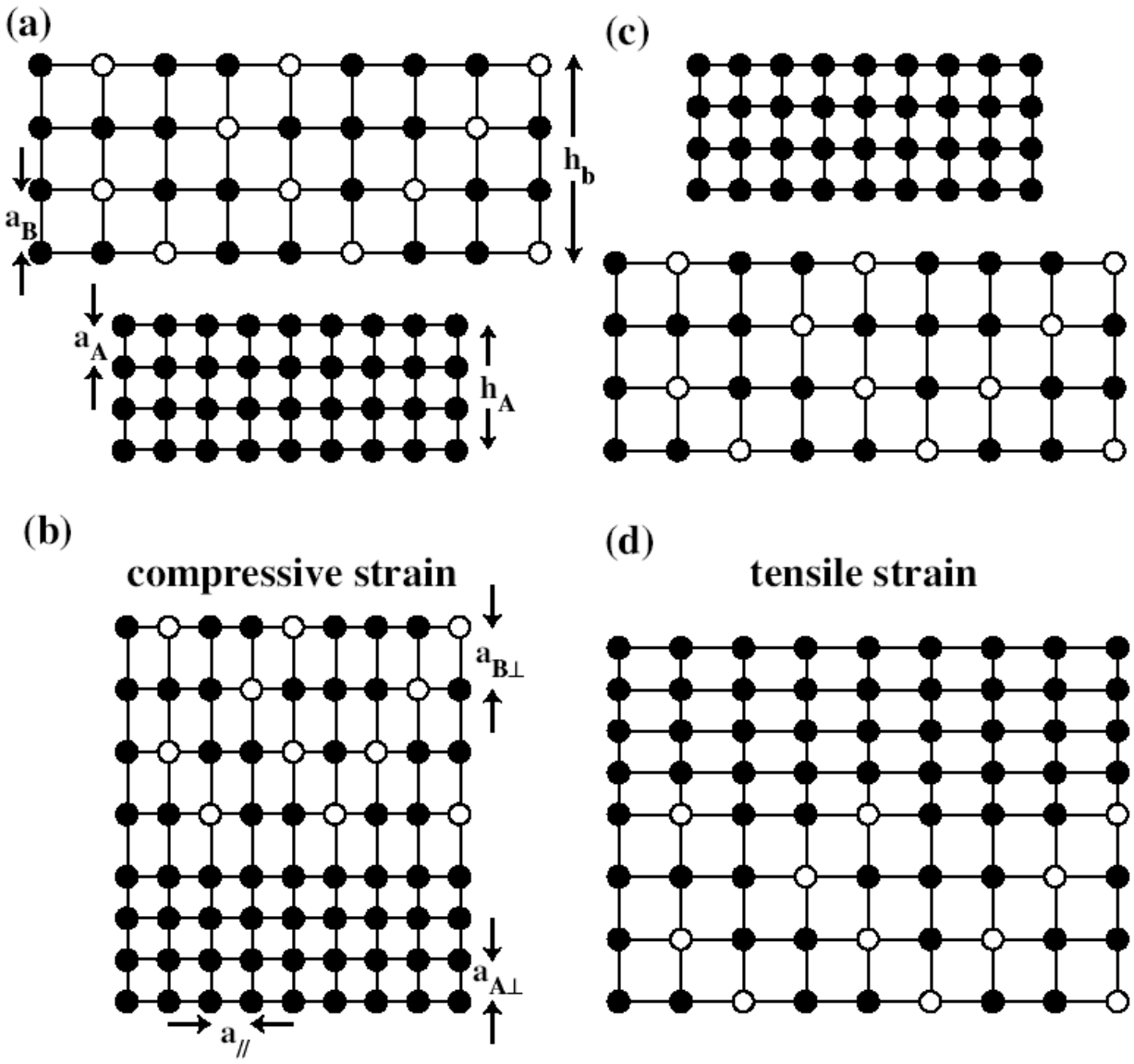

Strain (%)
0.0
0.50
1.0
1.5
2.0
Electron mobility enhancement
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
IBM theory
+ experiment
Fossum theory
Rashed
theory
Oberhaus theory
Takagi theory
0
10
20
30
40
50
Ge content (%)

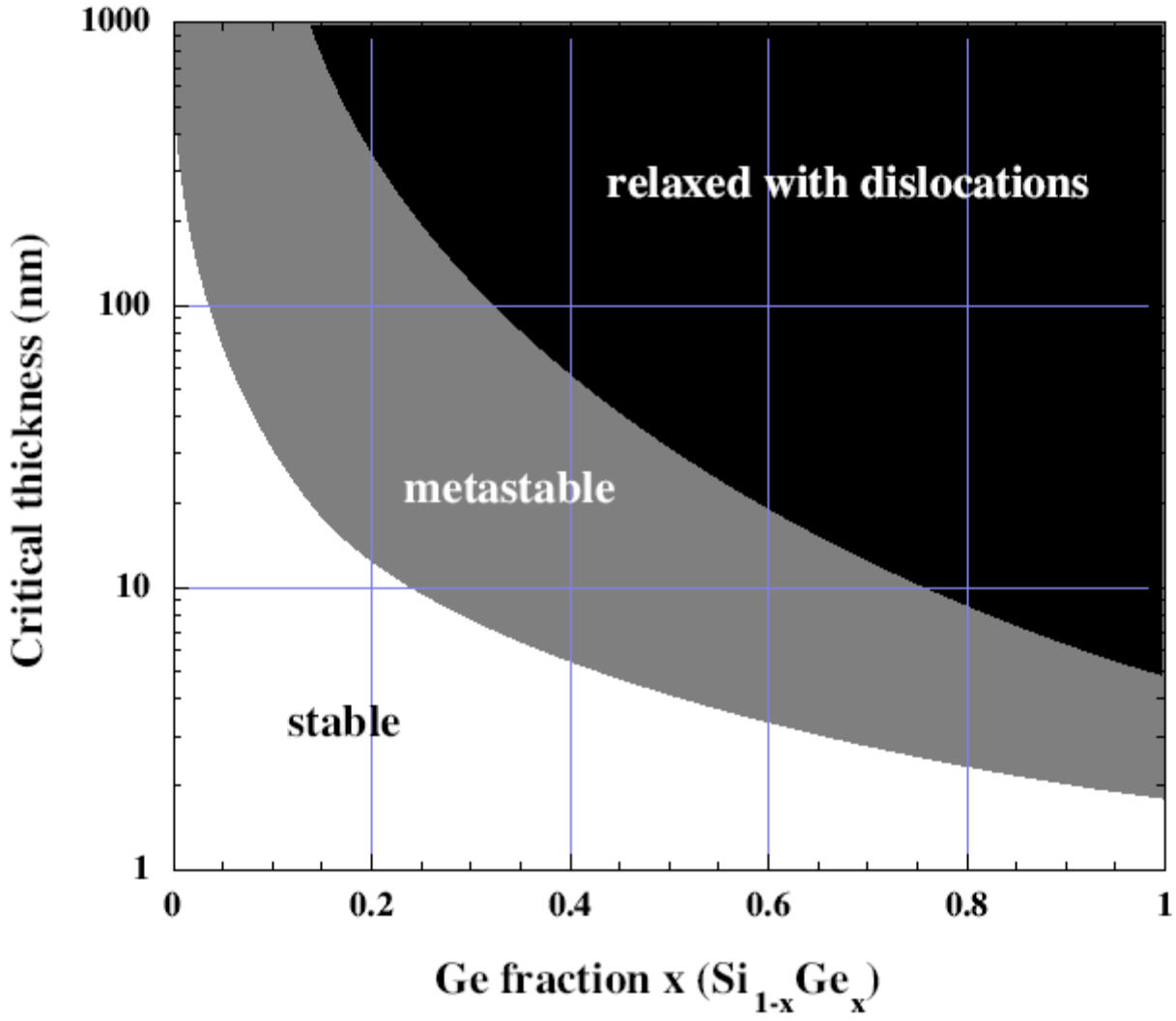

Effective electron mobility (cm²/Vs)
800
700
600
500
400
300
200
100
0
0
0.5
1
1.5
2
Vertical effective field, E_eff (MV/cm)
universal mobility
Rim 20% Ge
Hitachi 30% Ge
IBM SSOI 15% Ge
IBM 20%Ge
IBM 15%Ge
IBM bulk Si


Strain (%)
0.0
0.50
1.0
1.5
2.0
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
hole mobility enhancement
Fossum theory (dashed)
Oberhaus theory
(solid)
IBM theory + experiment
0
10
20
30
40
50
Ge content (%)

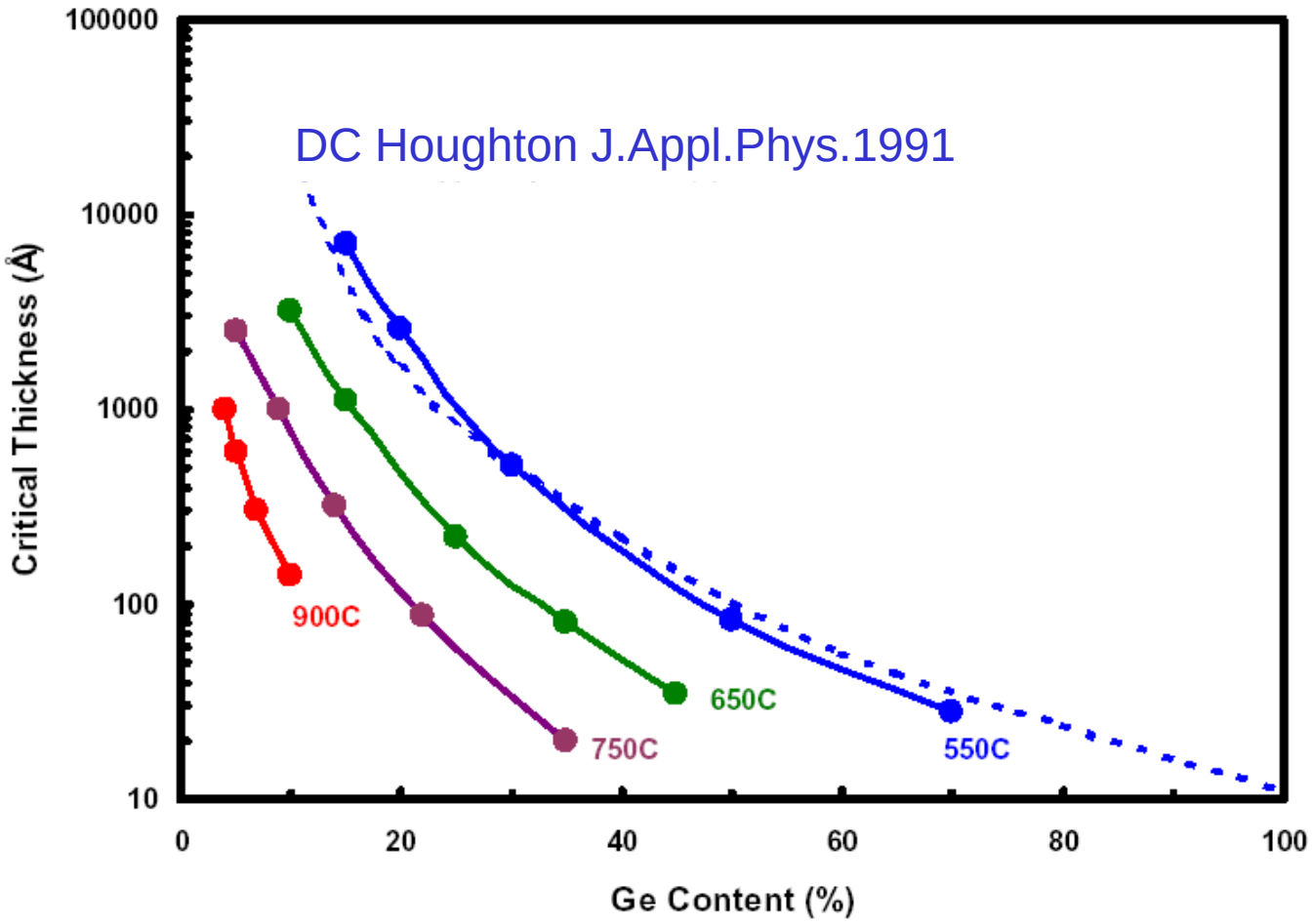
Intel's Strained Silicon Transistors

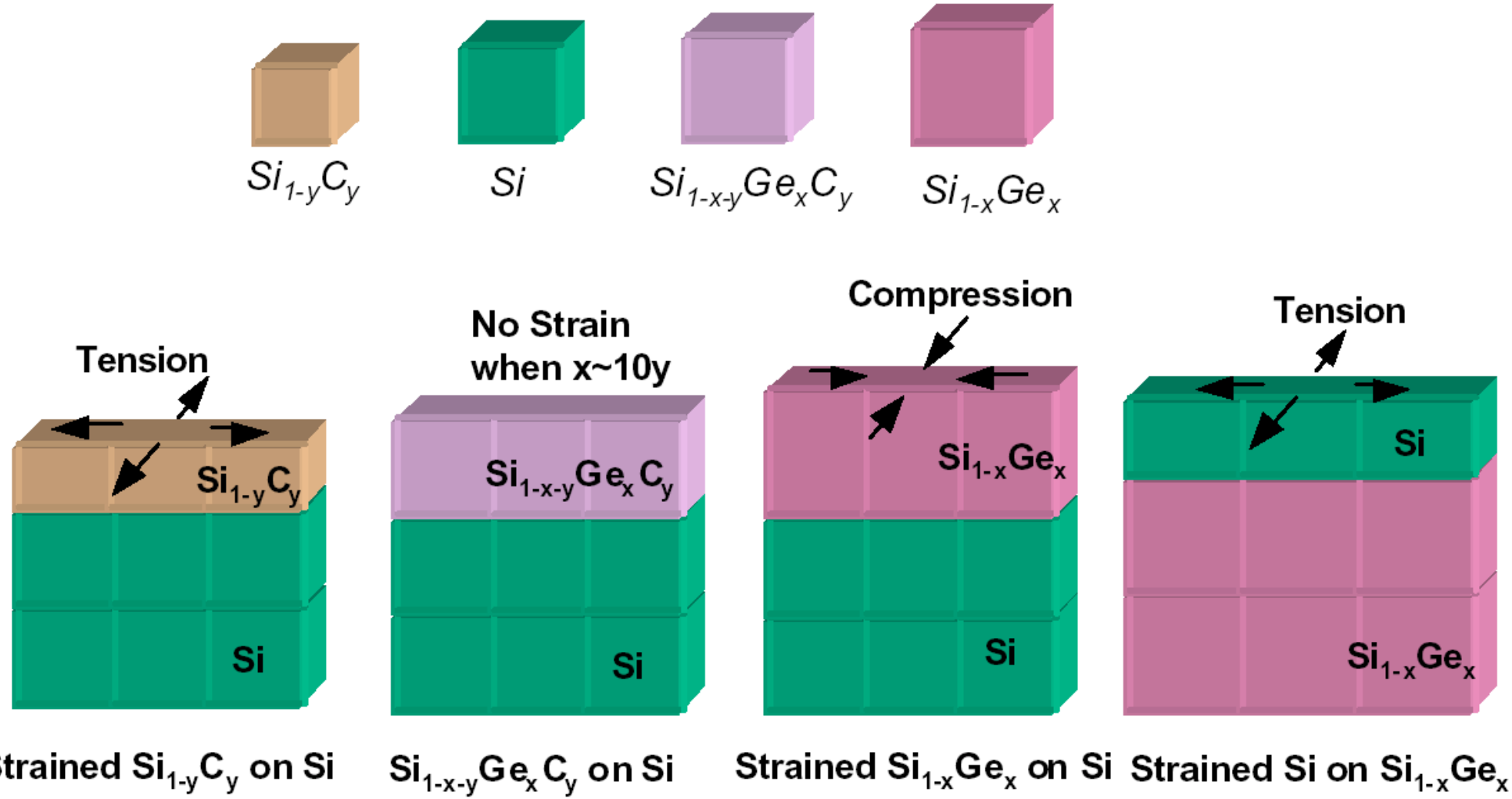



(a)
h_b
a_B
a_A
h_A
(c)
(b)
compressive strain
$a_{B\perp}$
$a_{A\perp}$
$a_{//}$
(d)
tensile strain


1000
100
10
1
Critical thickness (nm)
relaxed with dislocations
metastable
stable
0
0.2
0.4
0.6
0.8
1
Ge fraction x (Si1-xGex)

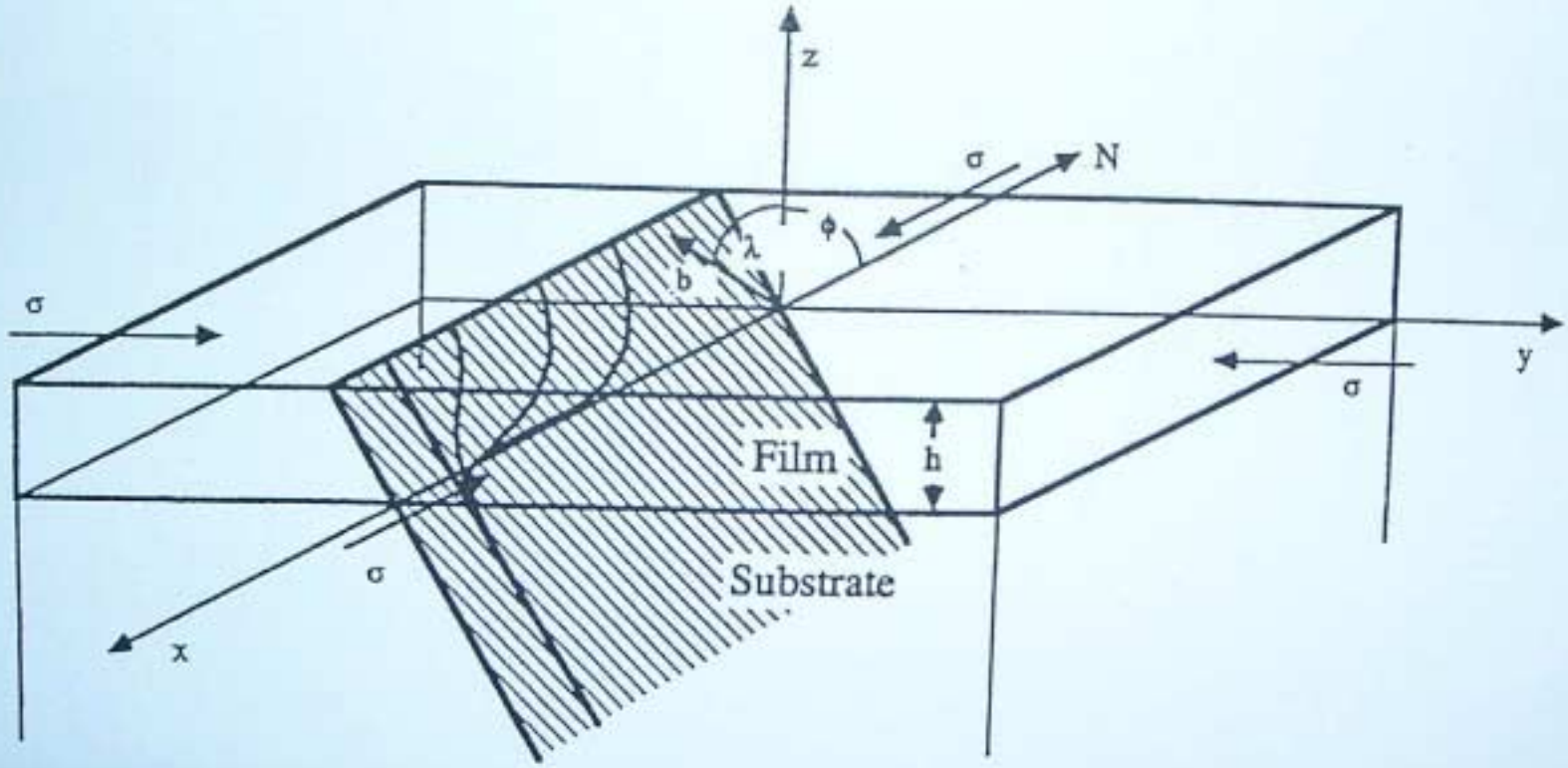
Critical Thickness for Pseudomorphic $Si_{1-x}Ge_x$




$Si_{1-y}C_y$
Si
$Si_{1-x-y}Ge_xC_y$
$Si_{1-x}Ge_x$
Tension
$Si_{1-y}C_y$
Si
Strained $Si_{1-y}C_y$ on Si
No Strain
when x~10y
$Si_{1-x-y}Ge_xC_y$
Si
$Si_{1-x-y}Ge_xC_y$ on Si
Compression
$Si_{1-x}Ge_x$
Si
Strained $Si_{1-x}Ge_x$ on Si
Tension
Si
$Si_{1-x}Ge_x$
Strained Si on $Si_{1-x}Ge_x$

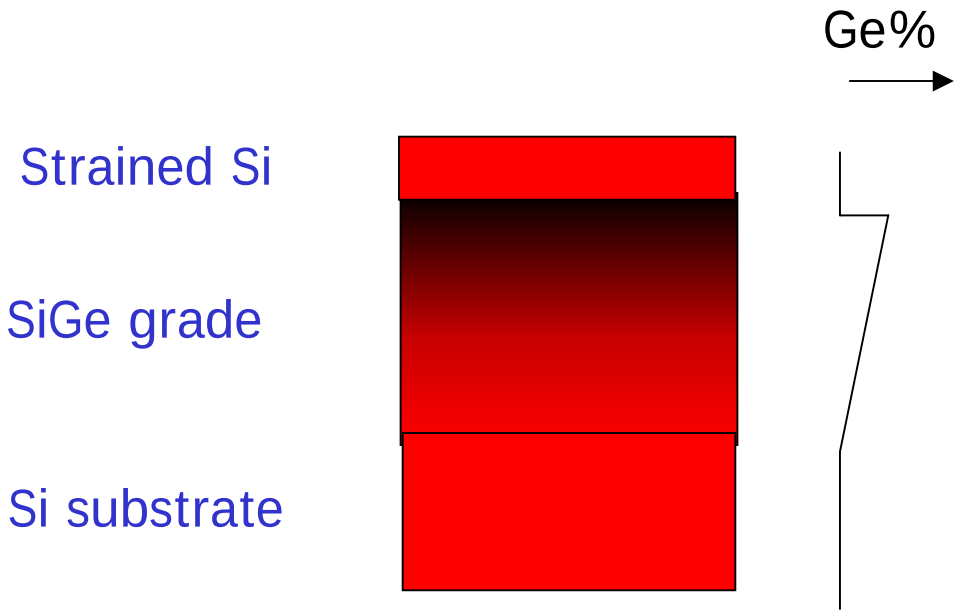
Formation of Misfit Dislocations

Dislocation Bending



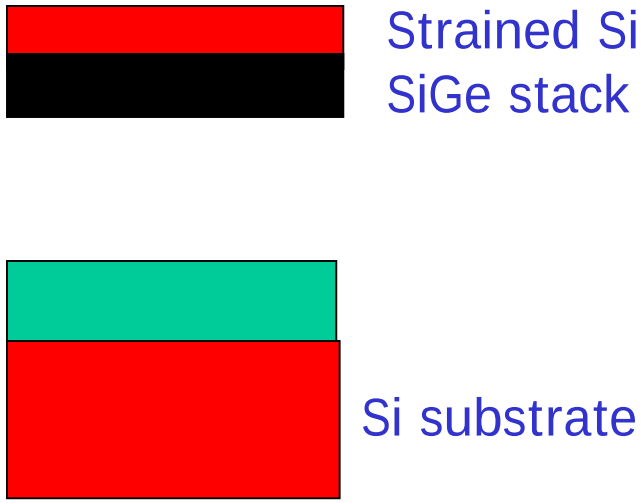
Strained Silicon on graded SiGe buffer

Amberwave

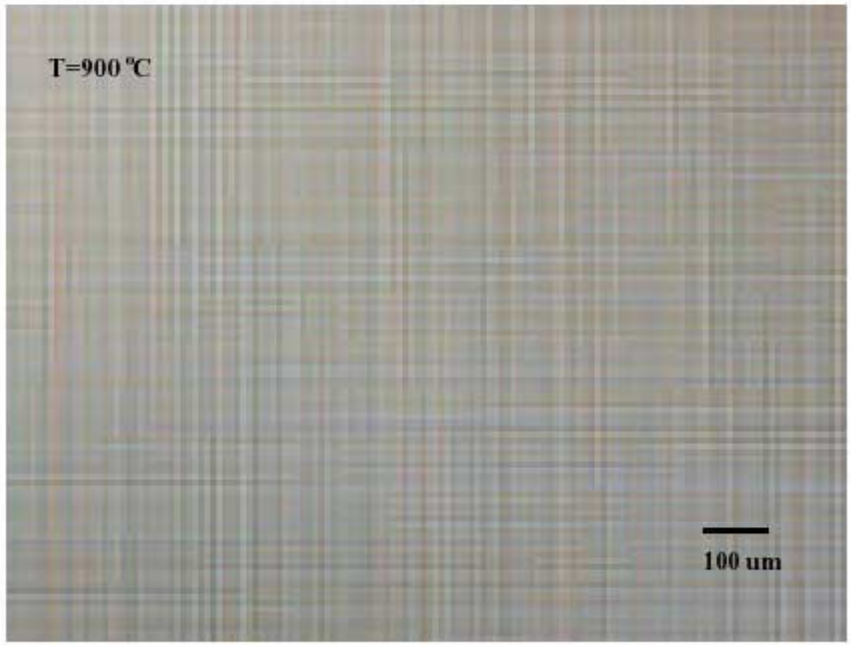


Strained Silicon on SOI wafer by layer transfer

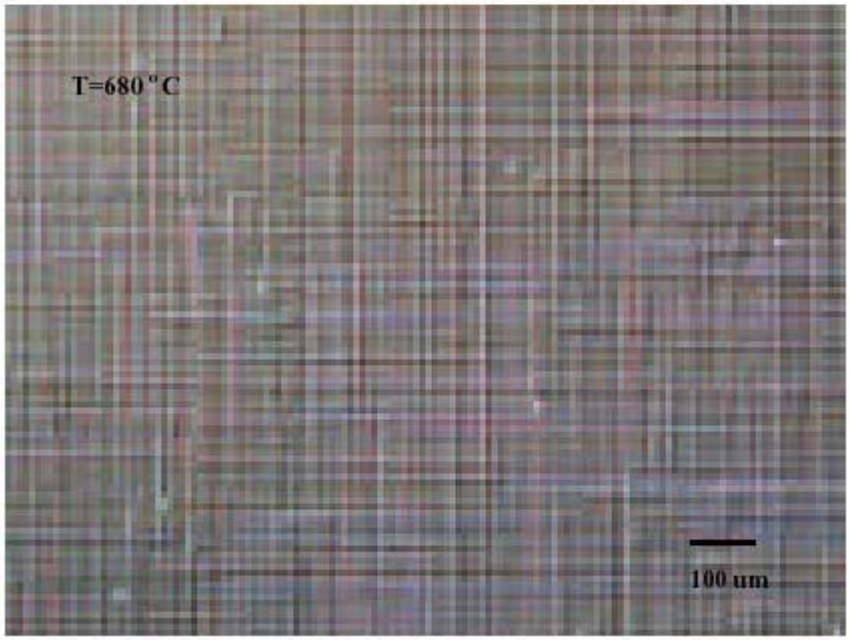
SOITEC

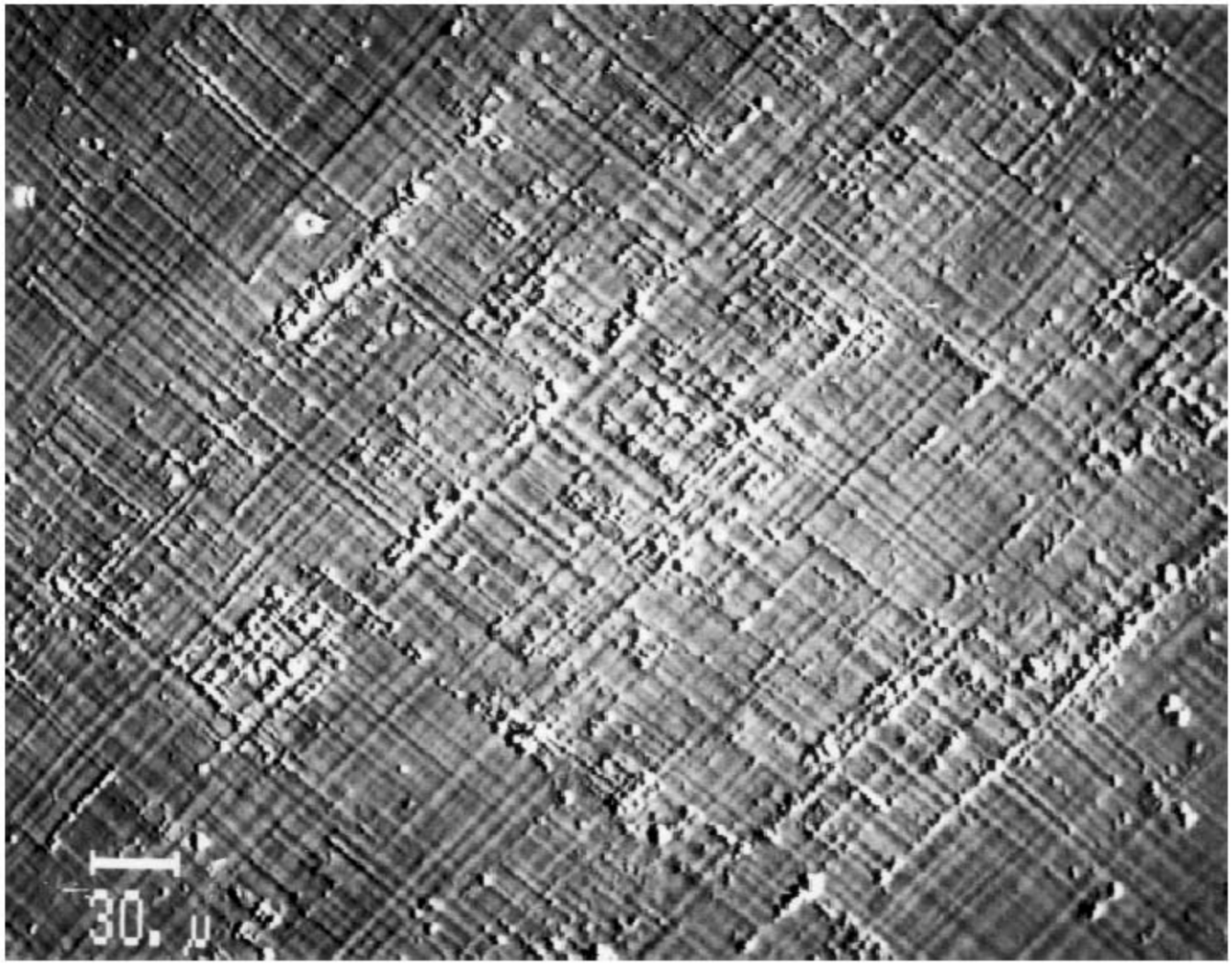


High Temperature Deposition

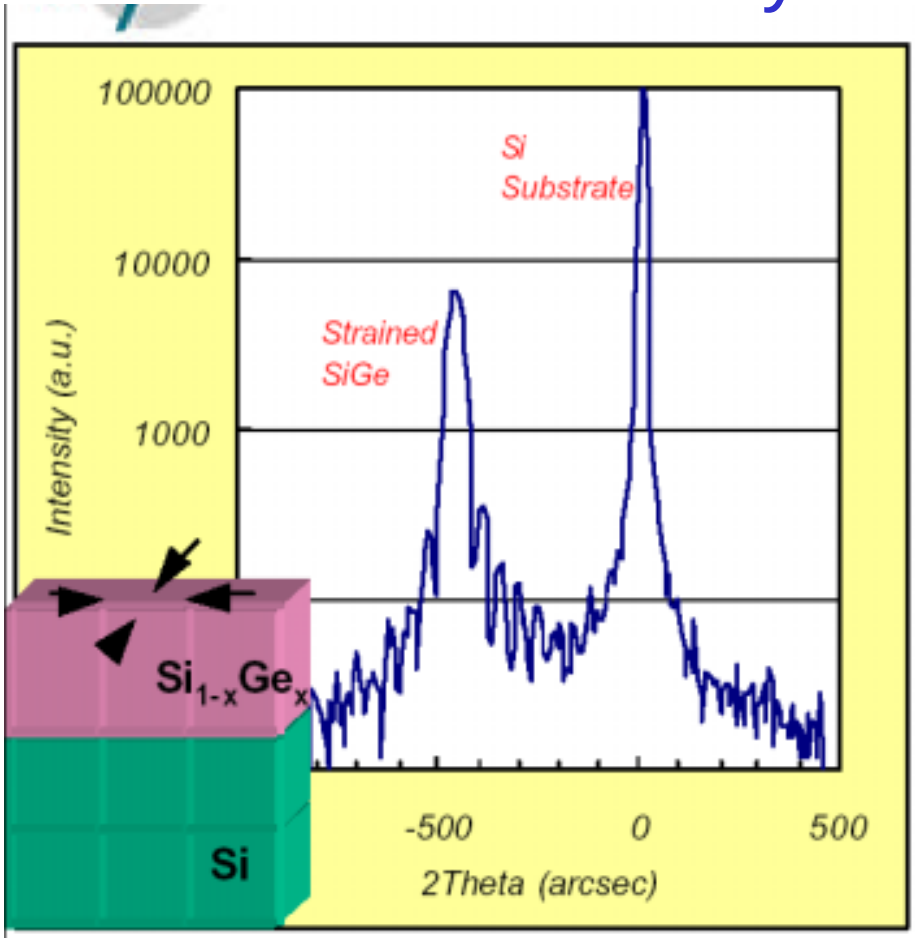


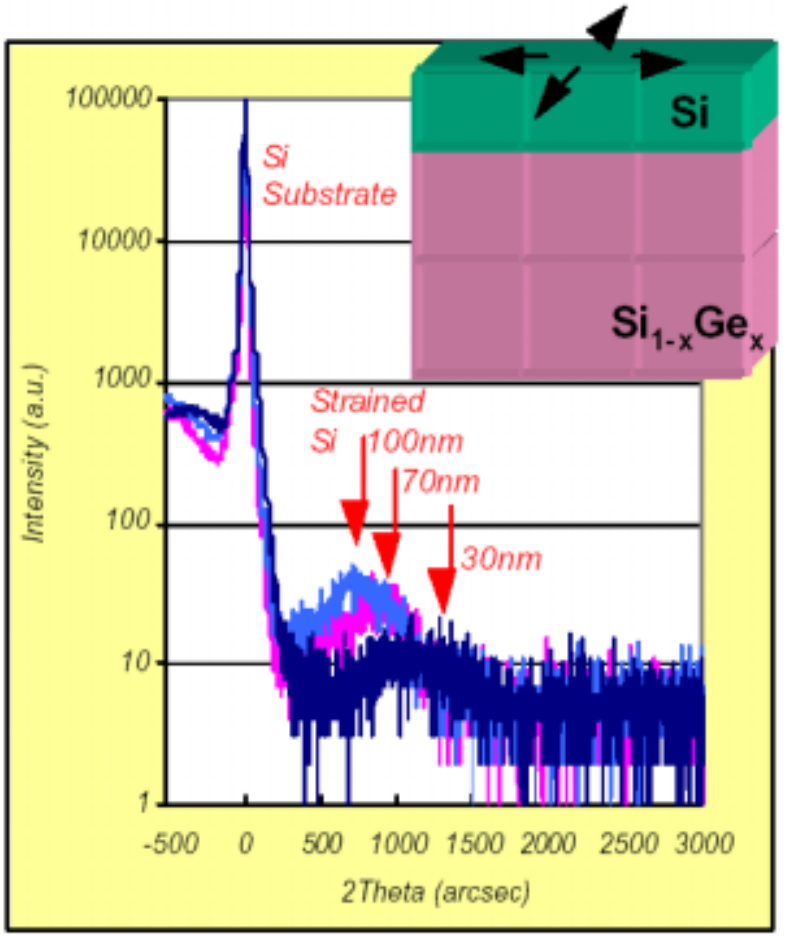
Low Temperature Deposition




30. µ

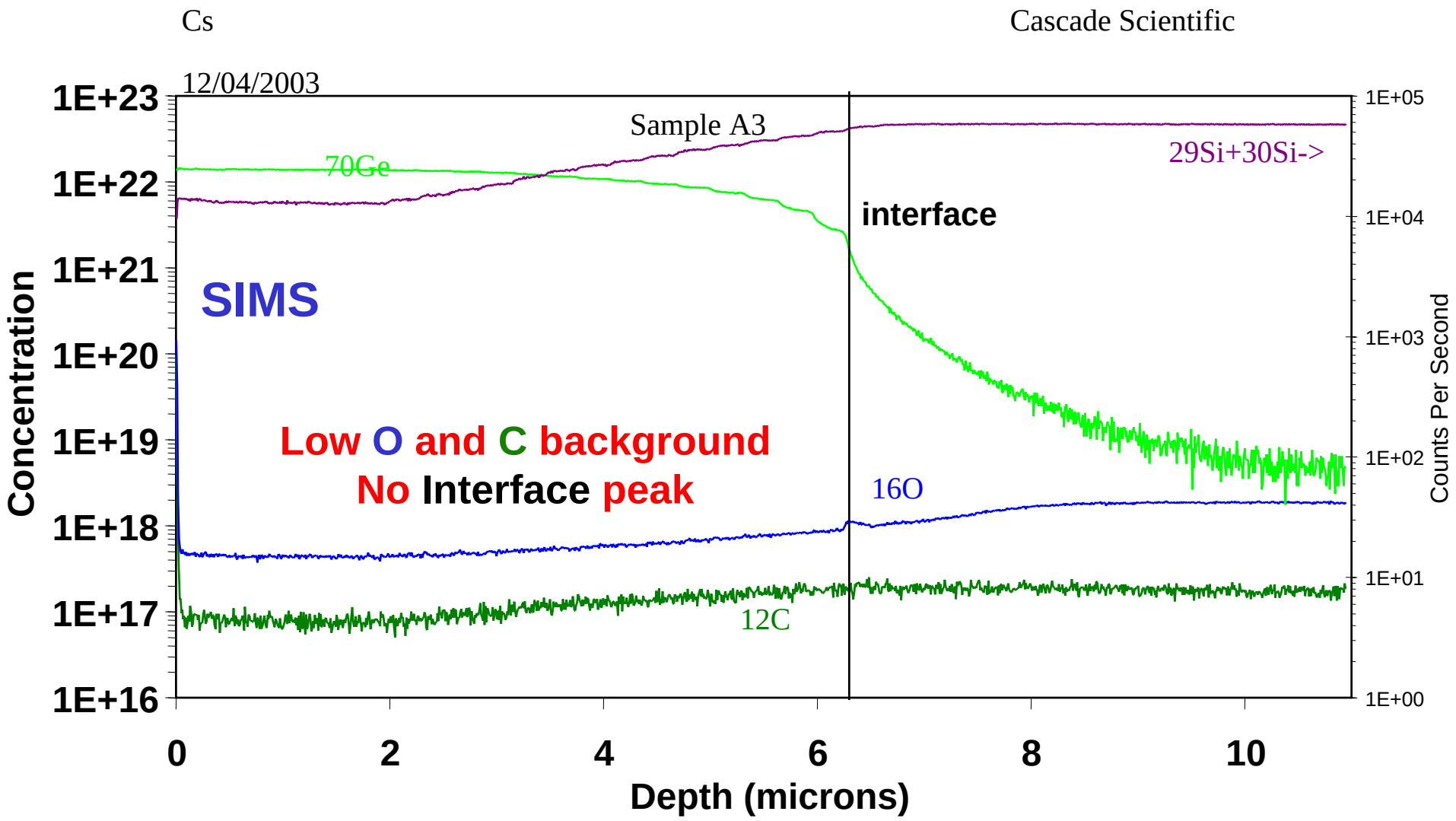
DCD x ray diffraction





Stress in Strained SiGe is Compressive. Stress in Strained Si is Tensile. Increasing the Si Thickness Above 300 Å Decreases the Strain and Shifts the Strained Si Peak Closer to the Substrate Peak.

SIMS profileStrained Si – Graded SiGe Buffer



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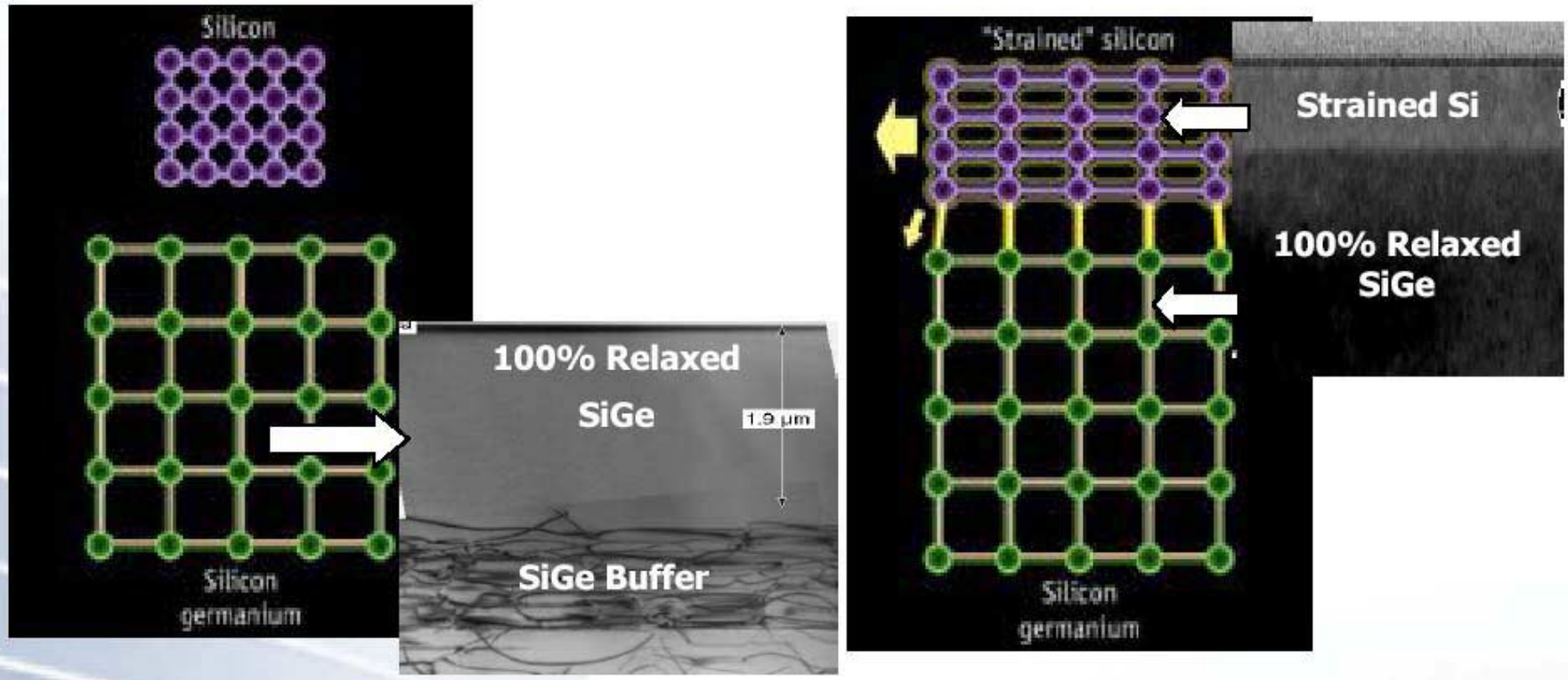
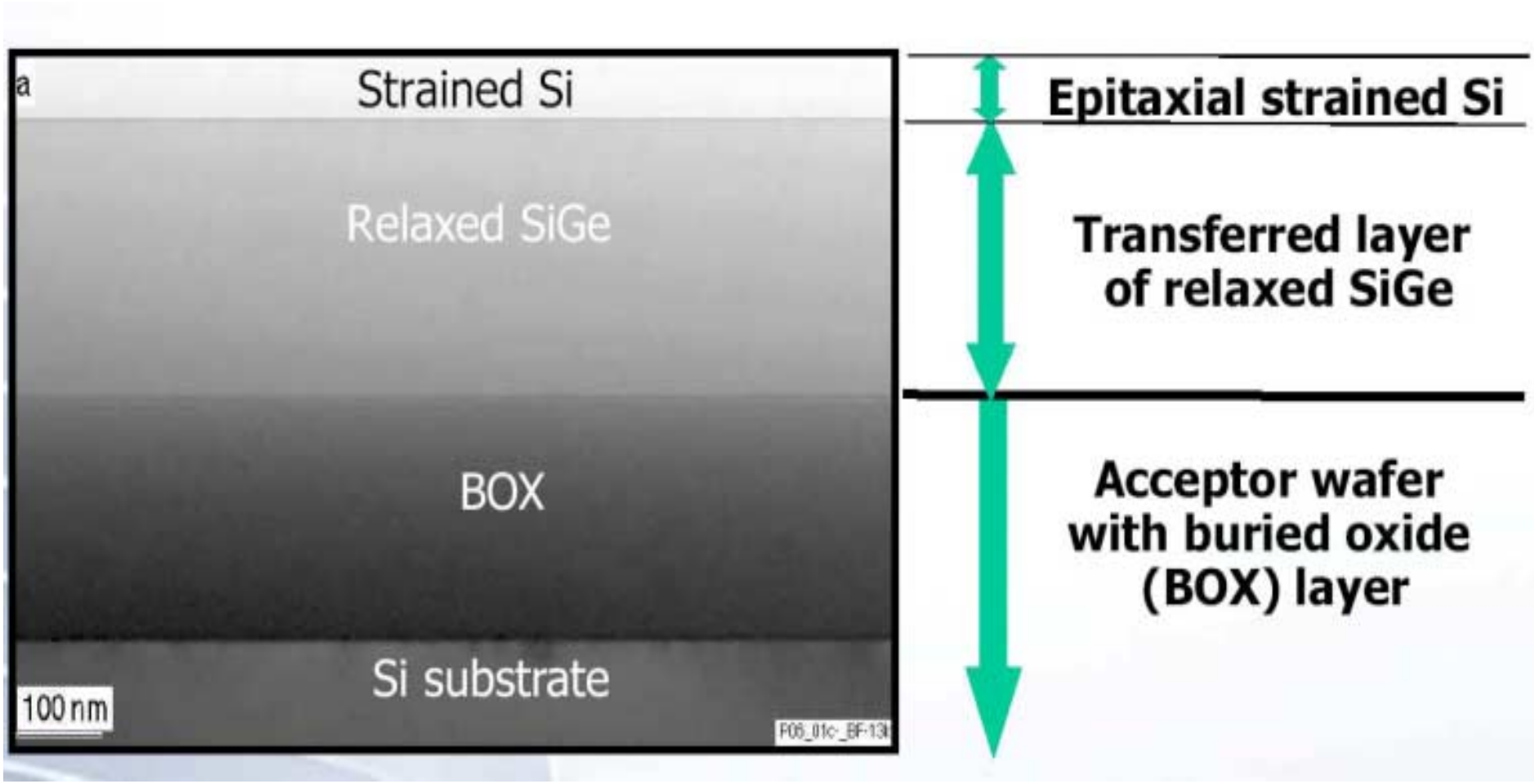
Principle for Production of Strained Si Film



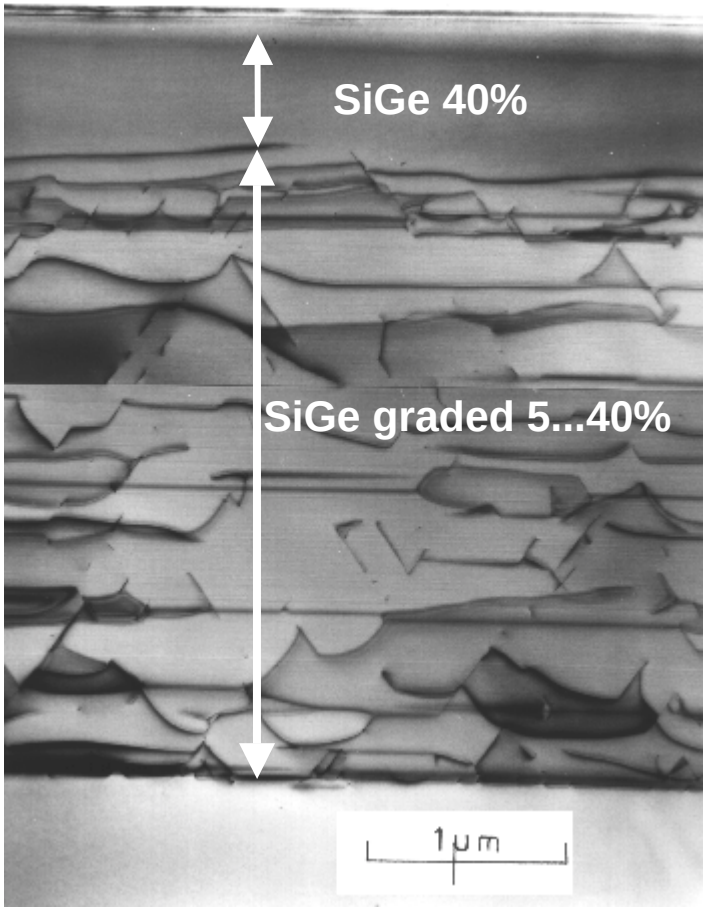
First a SiGe buffer layer is grown on Si followed by a relaxed SiGe layer with a lattice larger than Si

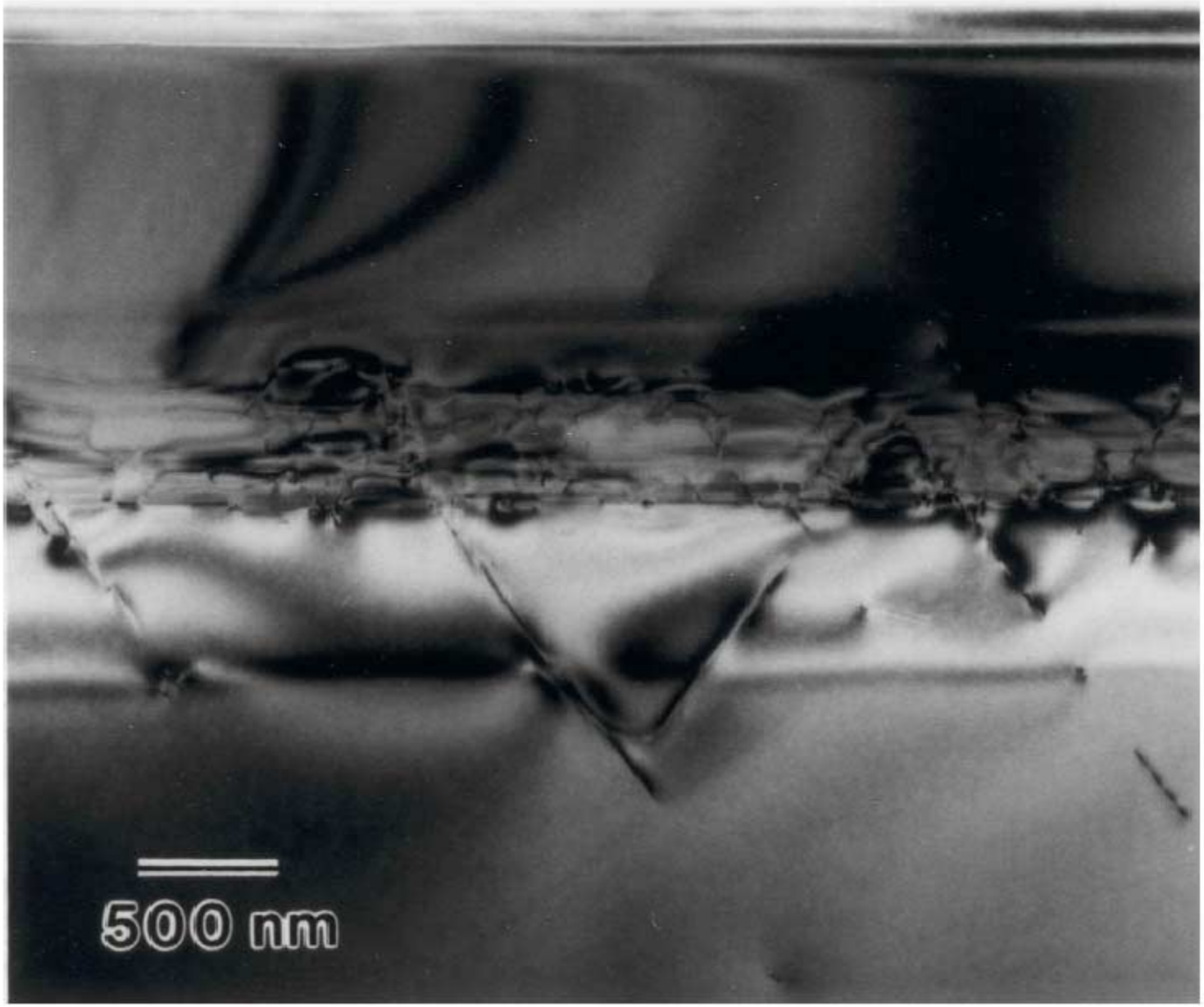
Next Si is grown on the relaxed SiGe layer; the Si atoms stretch to align with the SiGe layer so that the silicon layer becomes tensely strained

Graphs courtesy of IBM


a
Strained Si
Relaxed SiGe
BOX
Si substrate
100 nm
Epitaxial strained Si
Transferred layer of relaxed SiGe
Acceptor wafer with buried oxide (BOX) layer

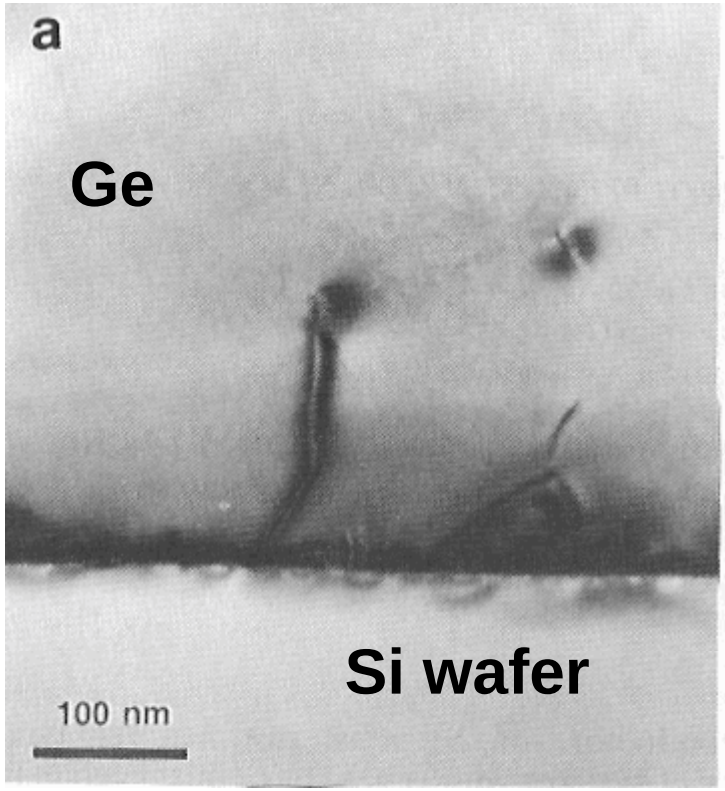
Strained Si layers

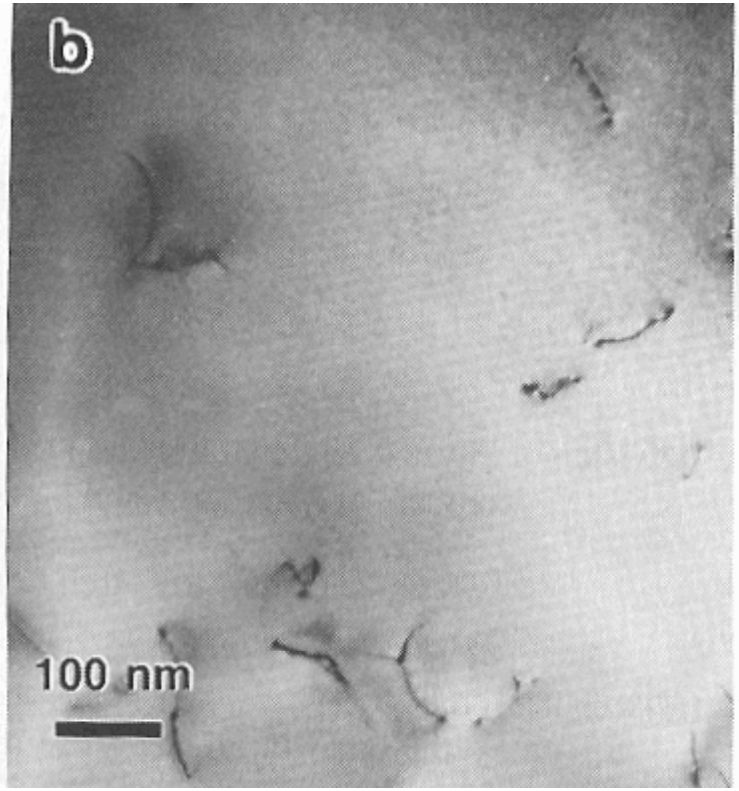



500 nm

Pure Ge on Silicon substrates

Low defect density Ge without SiGe graded buffer

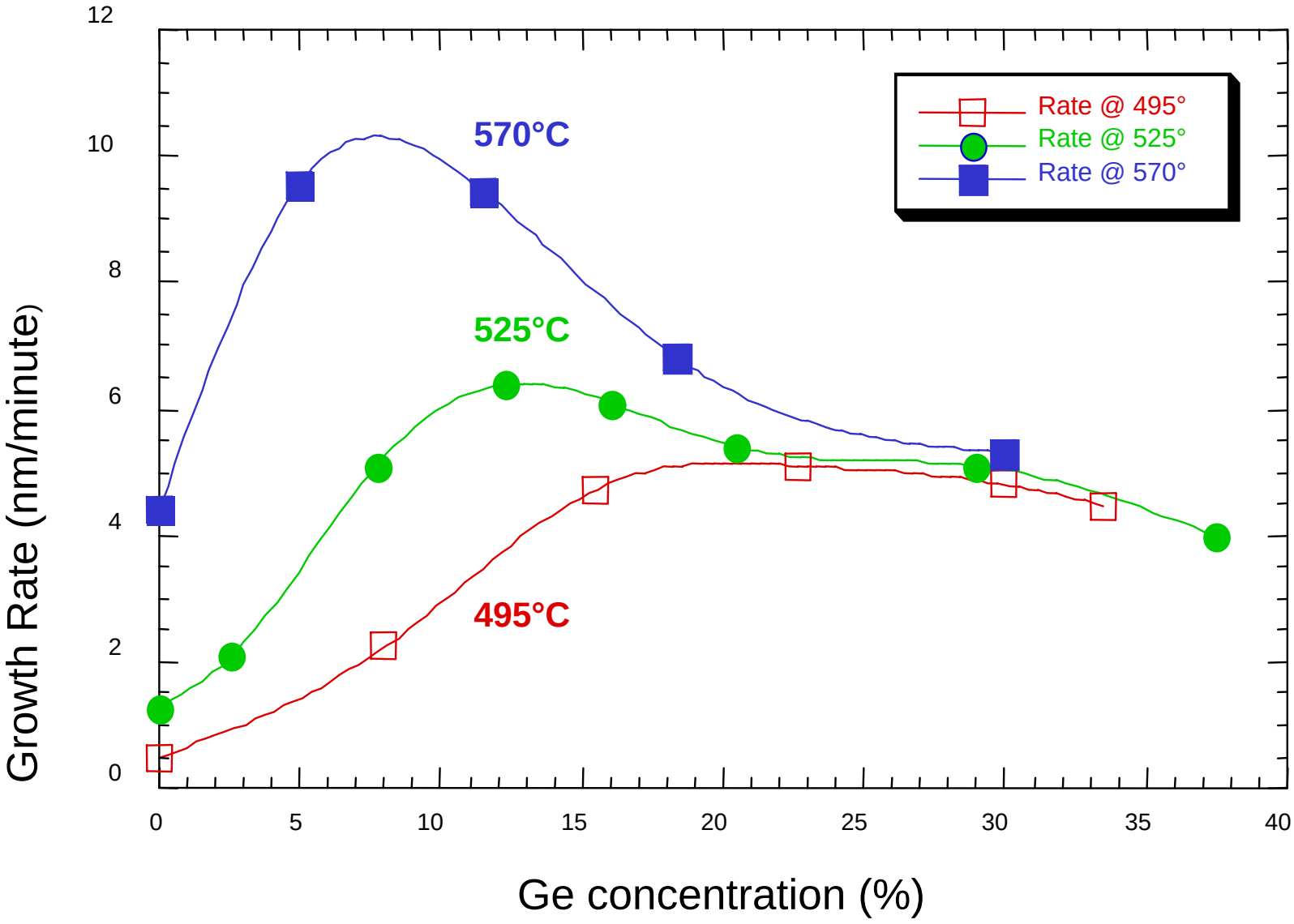




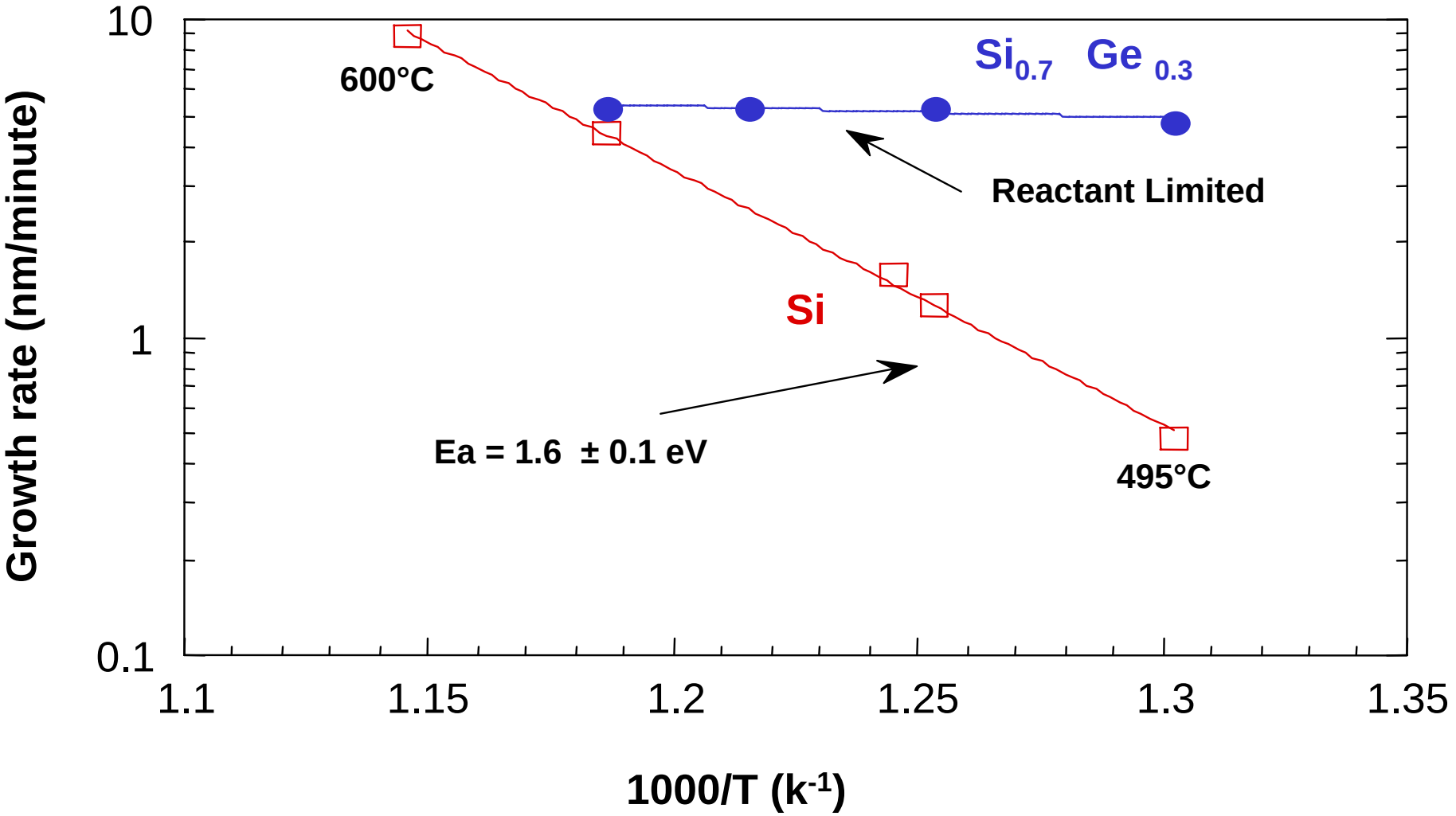
Cross sectional TEM

Plan view TEM (looking down through Ge cap)

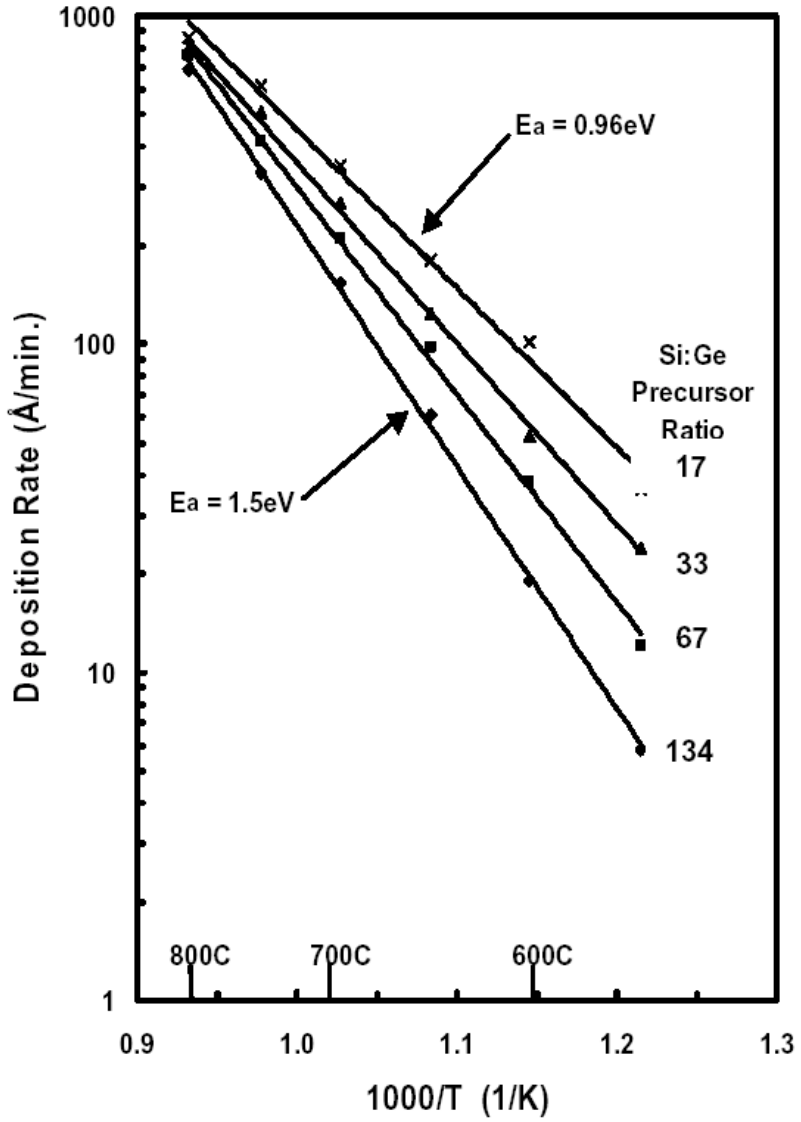
Growth Rate vs Germanium concentration

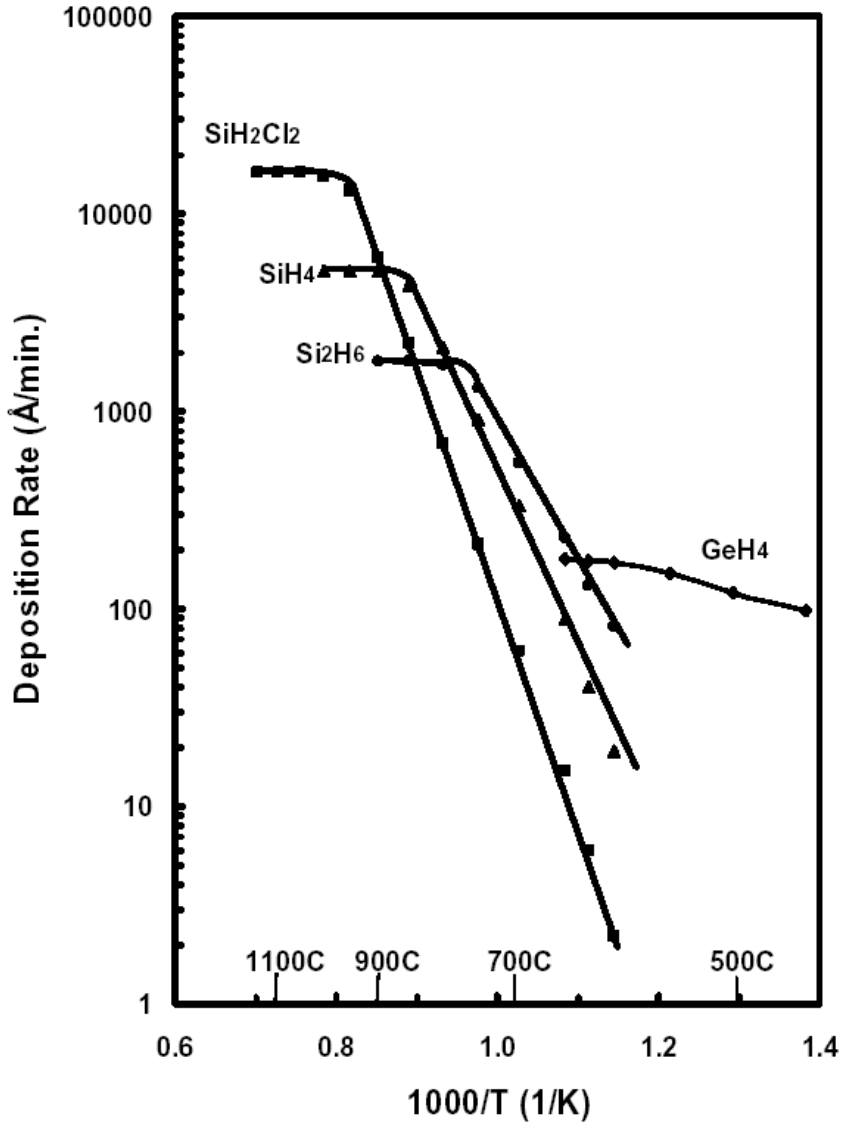


Growth Rates vs Temperature



Temperature Dependence of $Si_{1-x}Ge_x$ Deposition Rate





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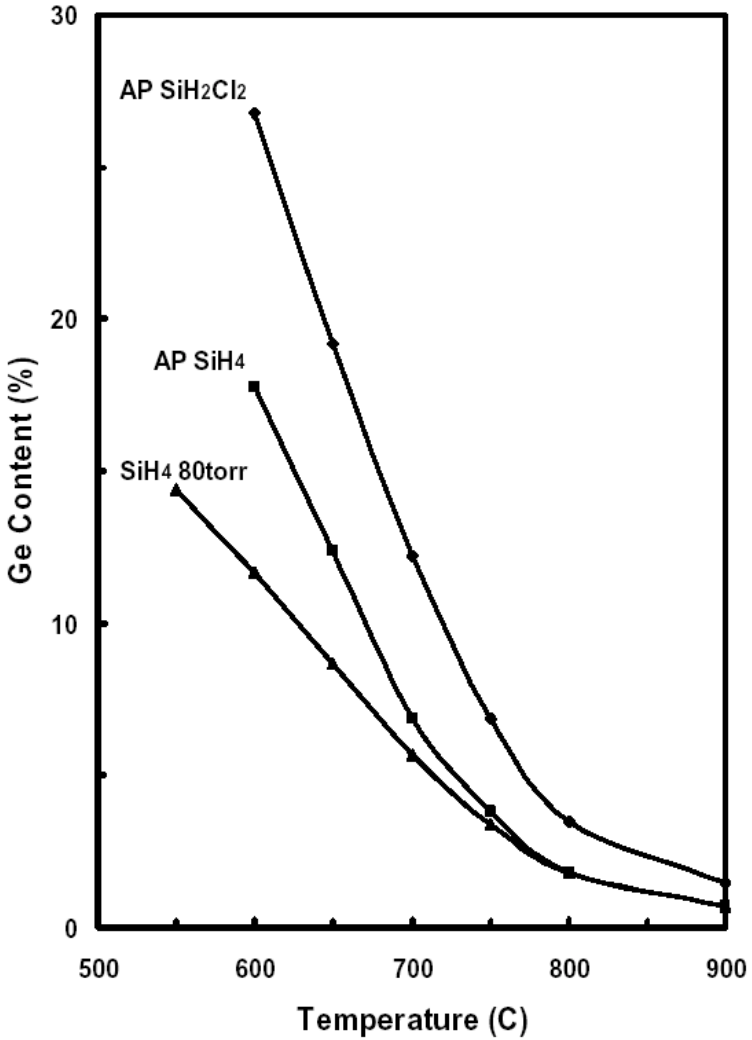
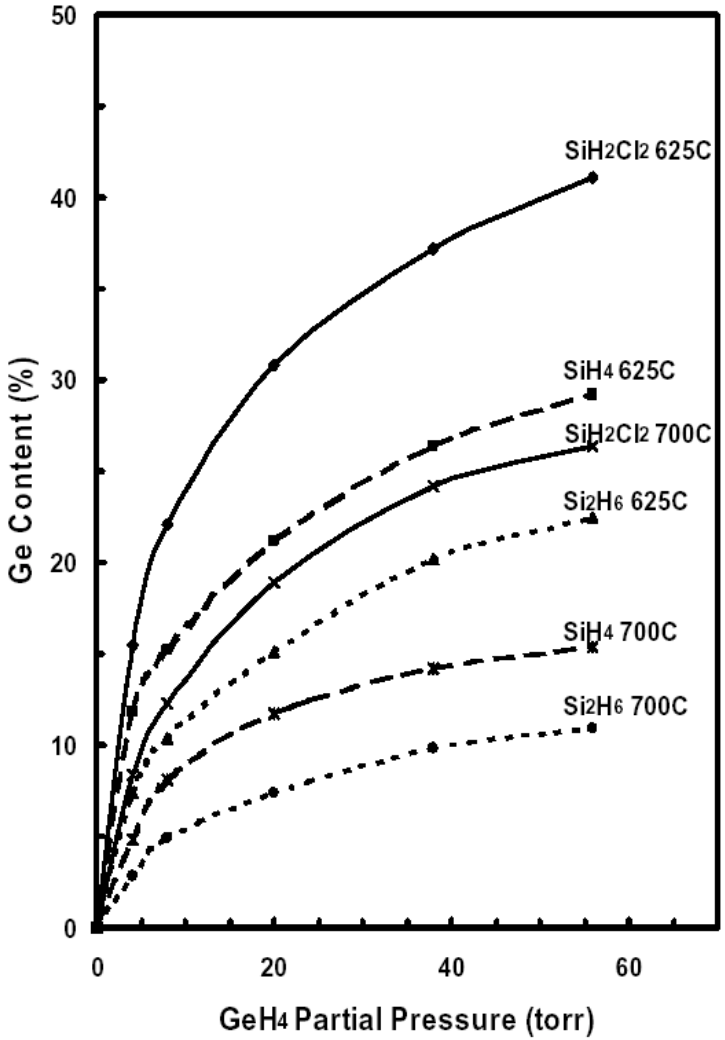
Effect of Temperature and GeH_4 on Ge Content





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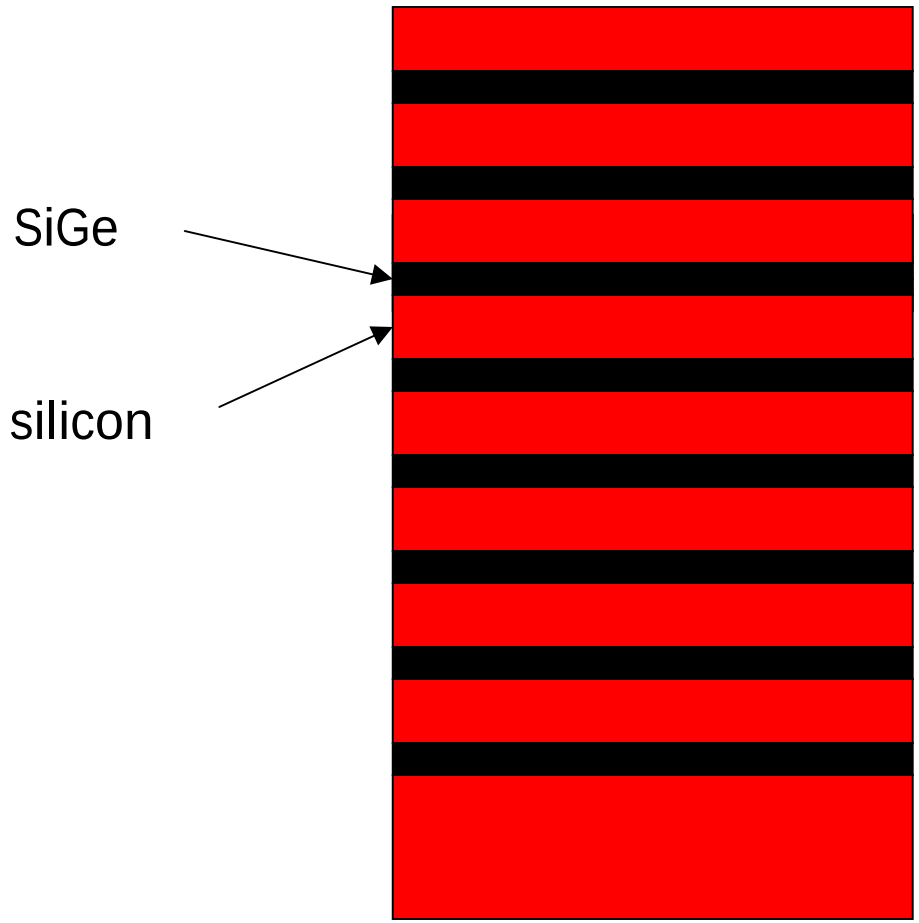
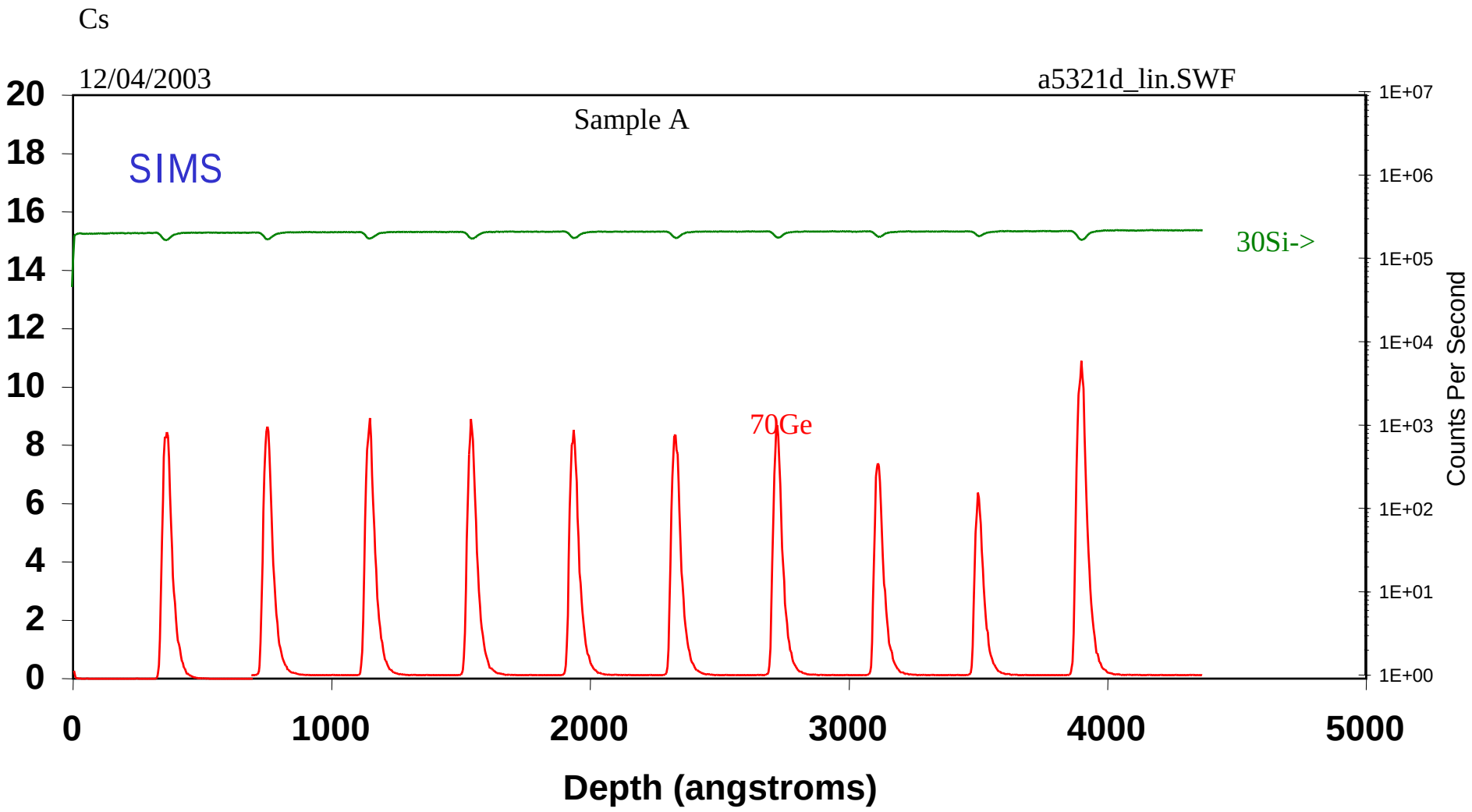
SiGe/Si Multilayer structure



Abrupt Si/SiGe interfaces and precise control of Ge % for “PIN Photodetector”

SiGe Multi Quantum Wells (MQW)



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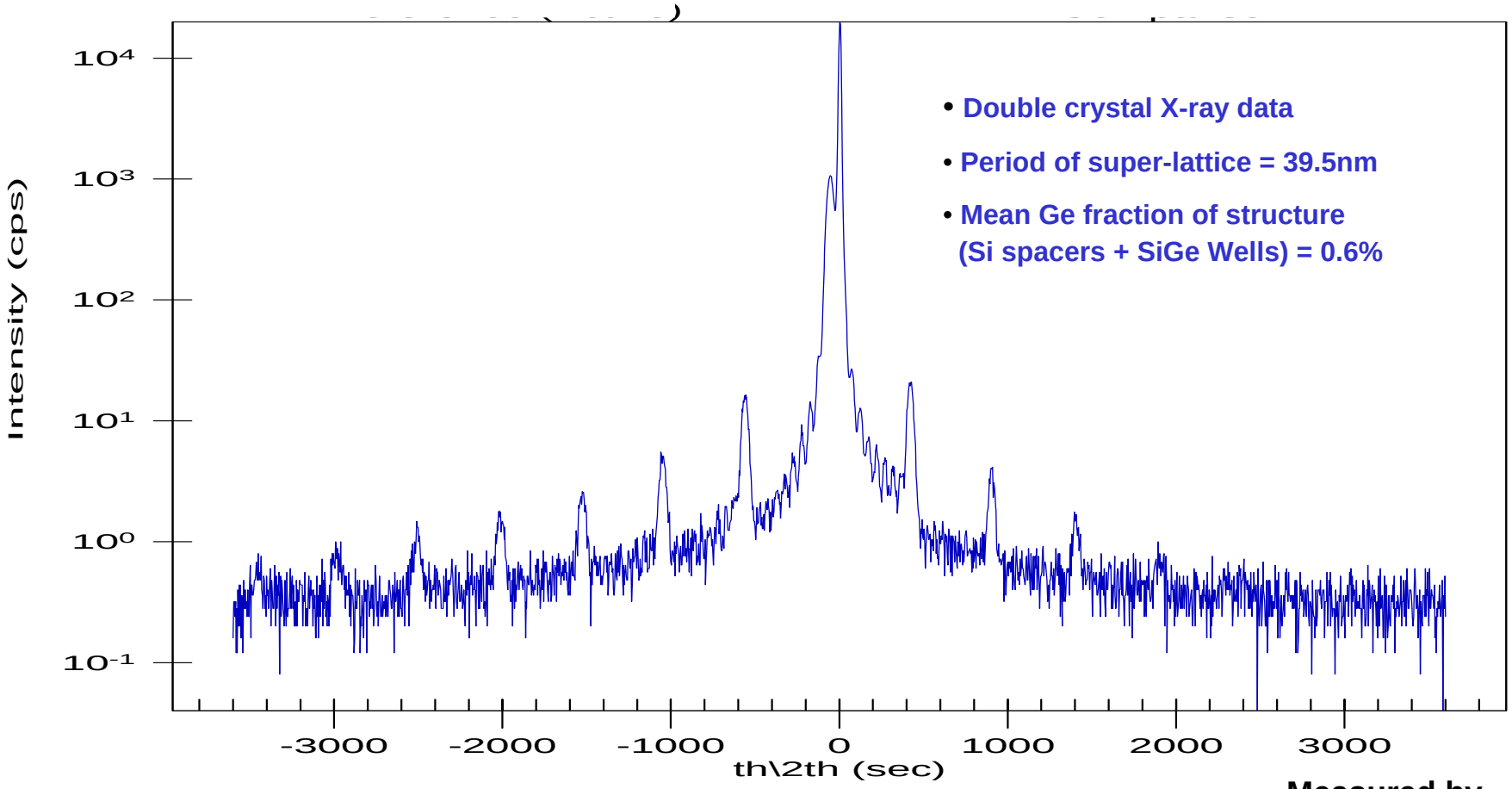
SiGe Multi Quantum Wells (MQW)



- Double crystal X-ray data
- Period of super-lattice = 39.5nm
- Mean Ge fraction of structure (Si spacers + SiGe Wells) = 0.6%

Measured by QinetiQ

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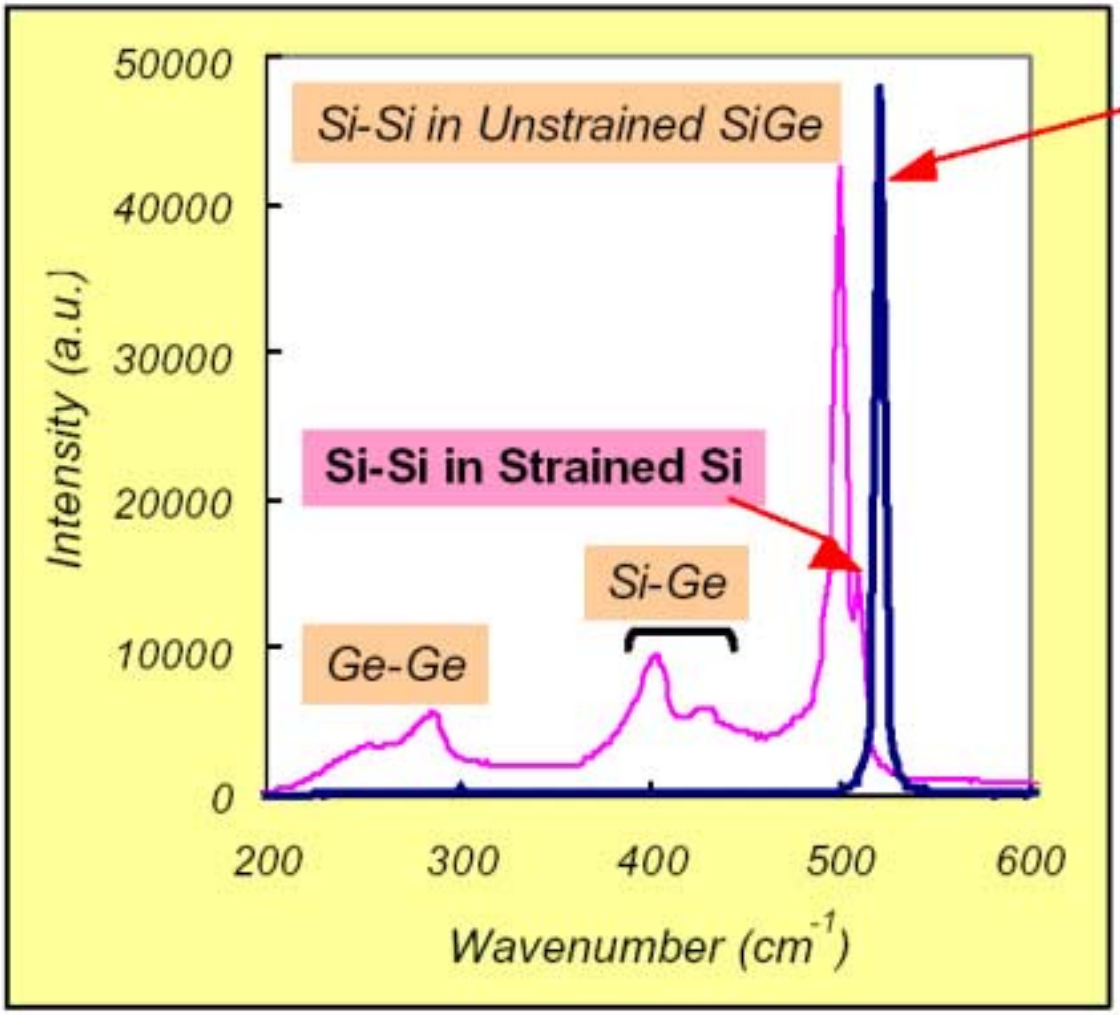
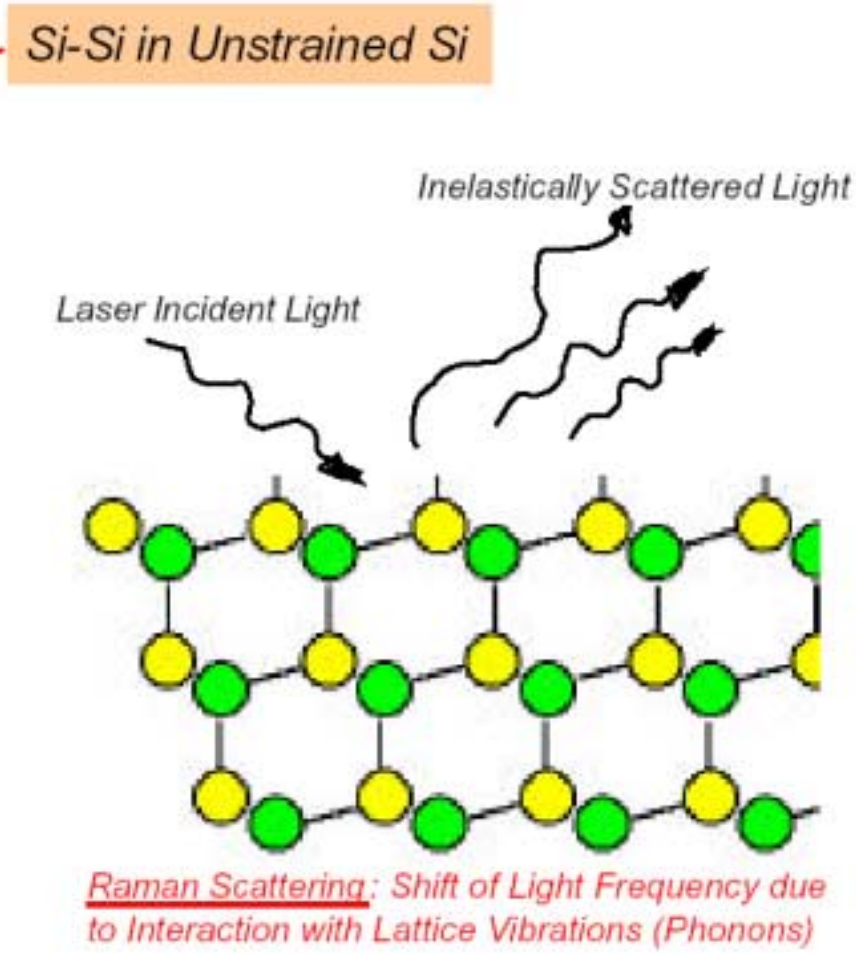
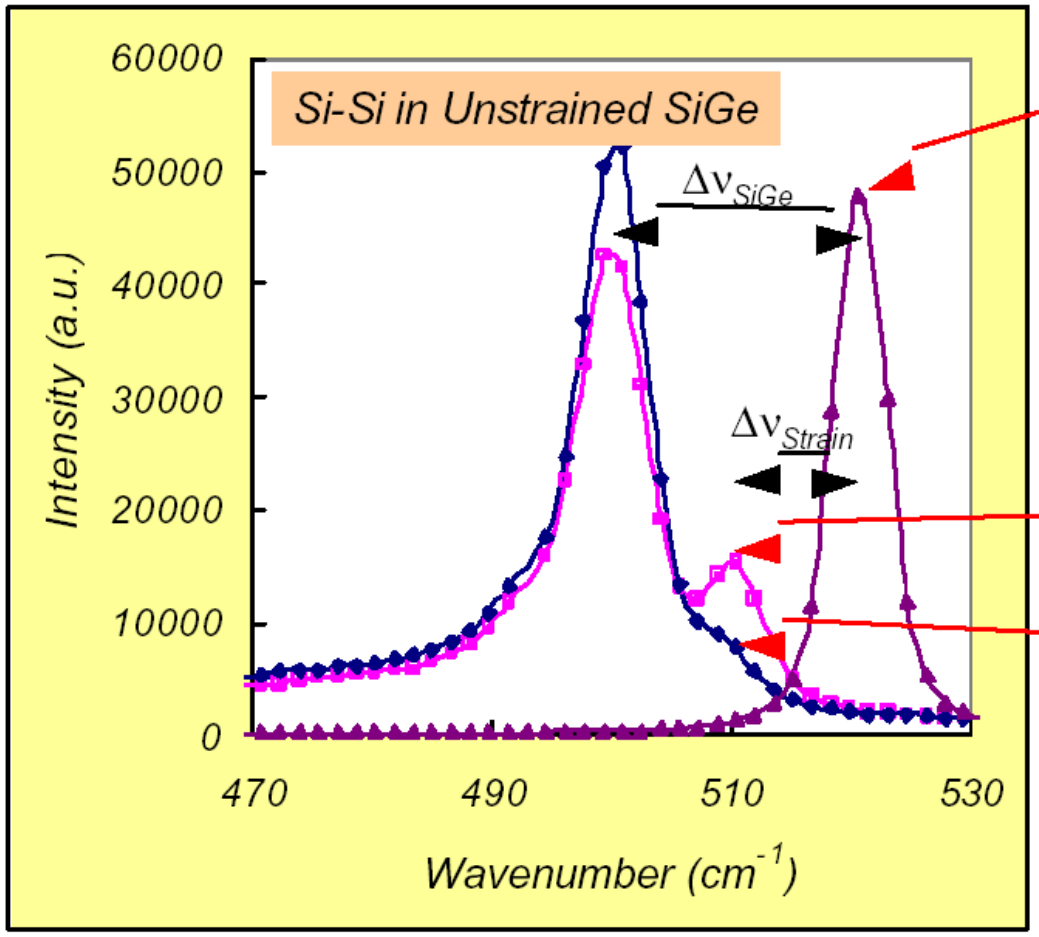
Raman Scattering





Raman Spectroscopy Can Provide Information on Molecular Vibrations of Lattice.

Raman Scattering



Si-Si in Unstrained Si

Si-Si Frequency Shift due to Strain σ

$\Delta\nu_{Strain} \approx -2 \cdot 10^{-9}\ \sigma$

Si-Si Frequency Shift due to x in $Si_{1-x}Ge_x$

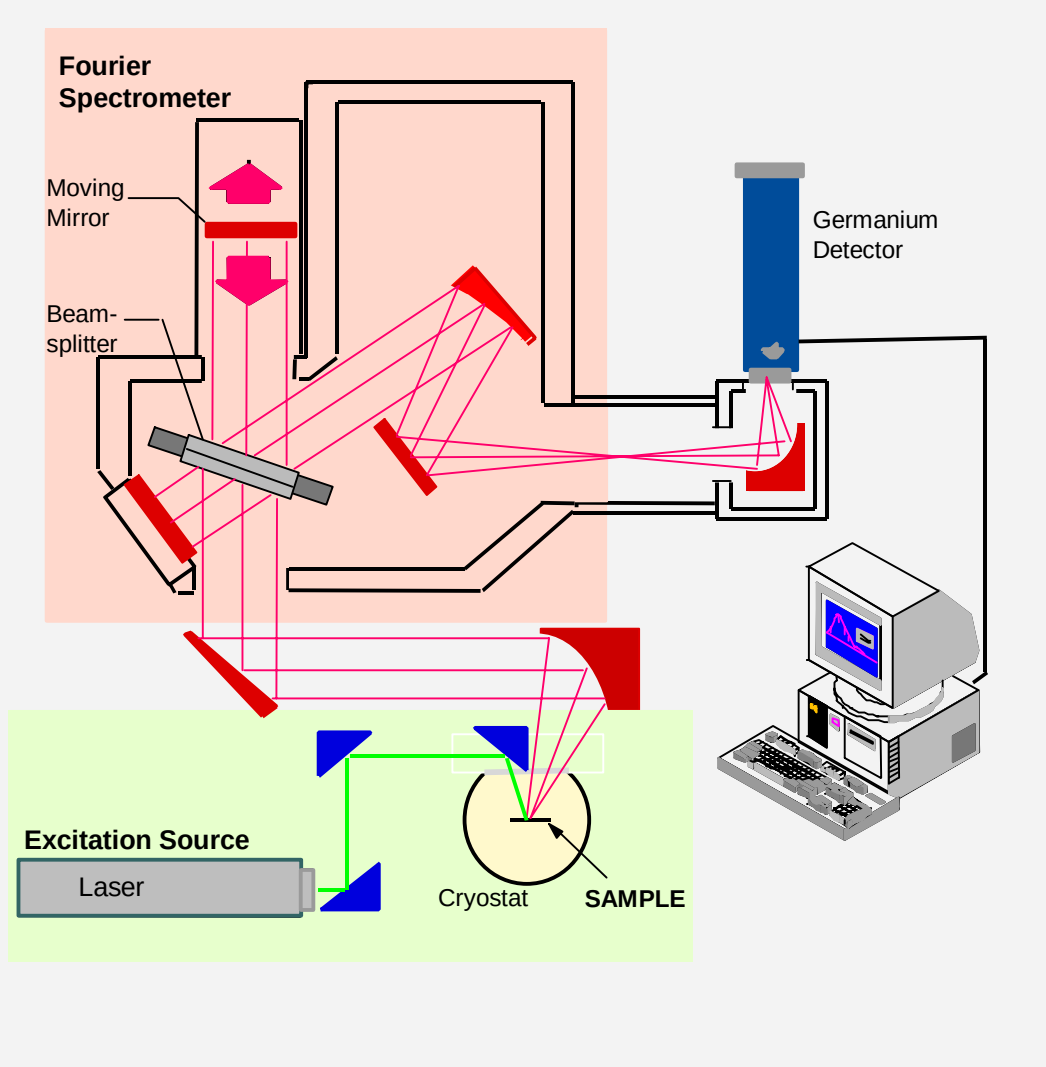
$\Delta\nu_{SiGe} = -70x$

Si-Si in 300Å Strained Si

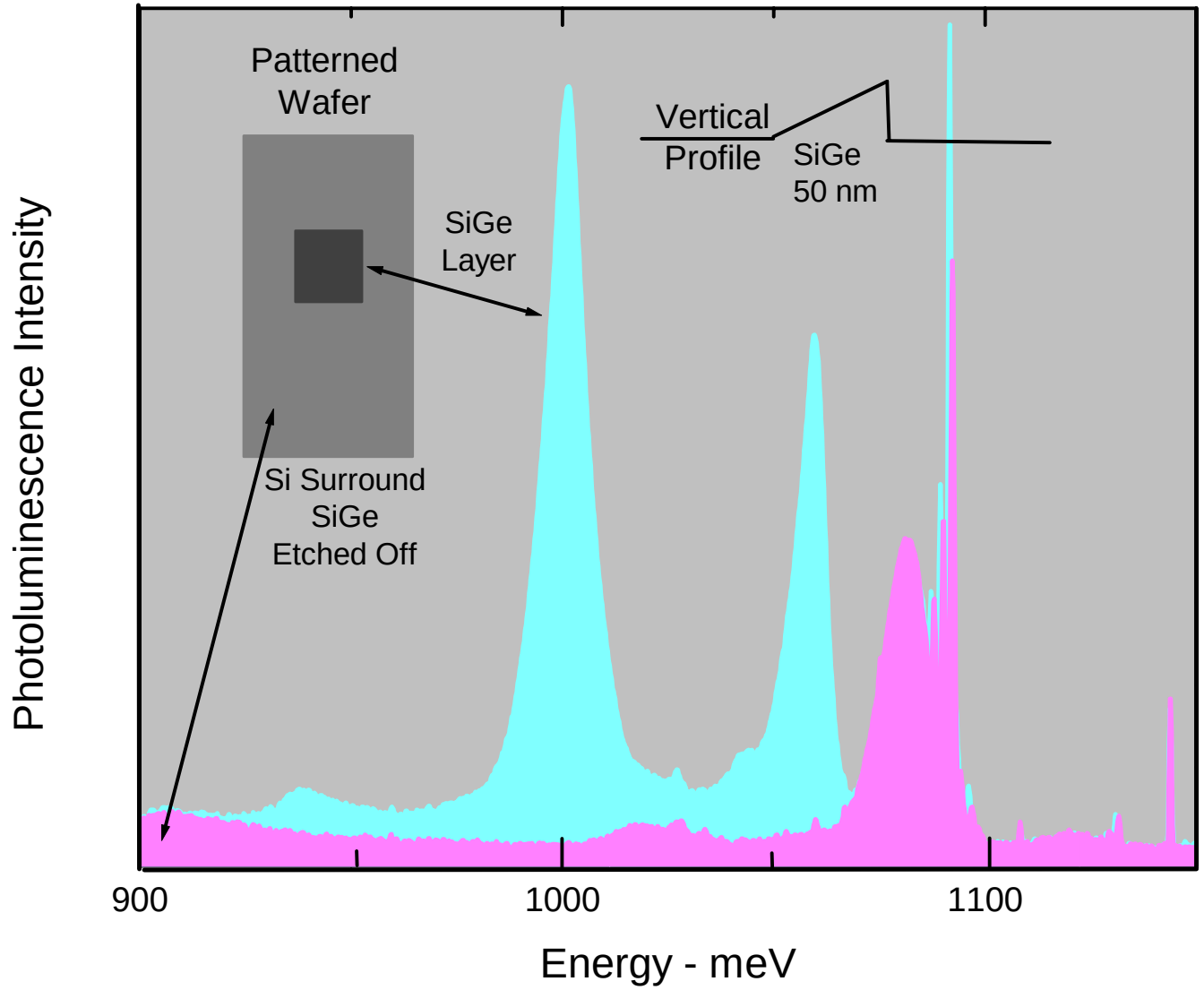
Si-Si in 100Å Strained Si

Tensile Stress in Strained Si is ~5 GPa (50,000 atm.).

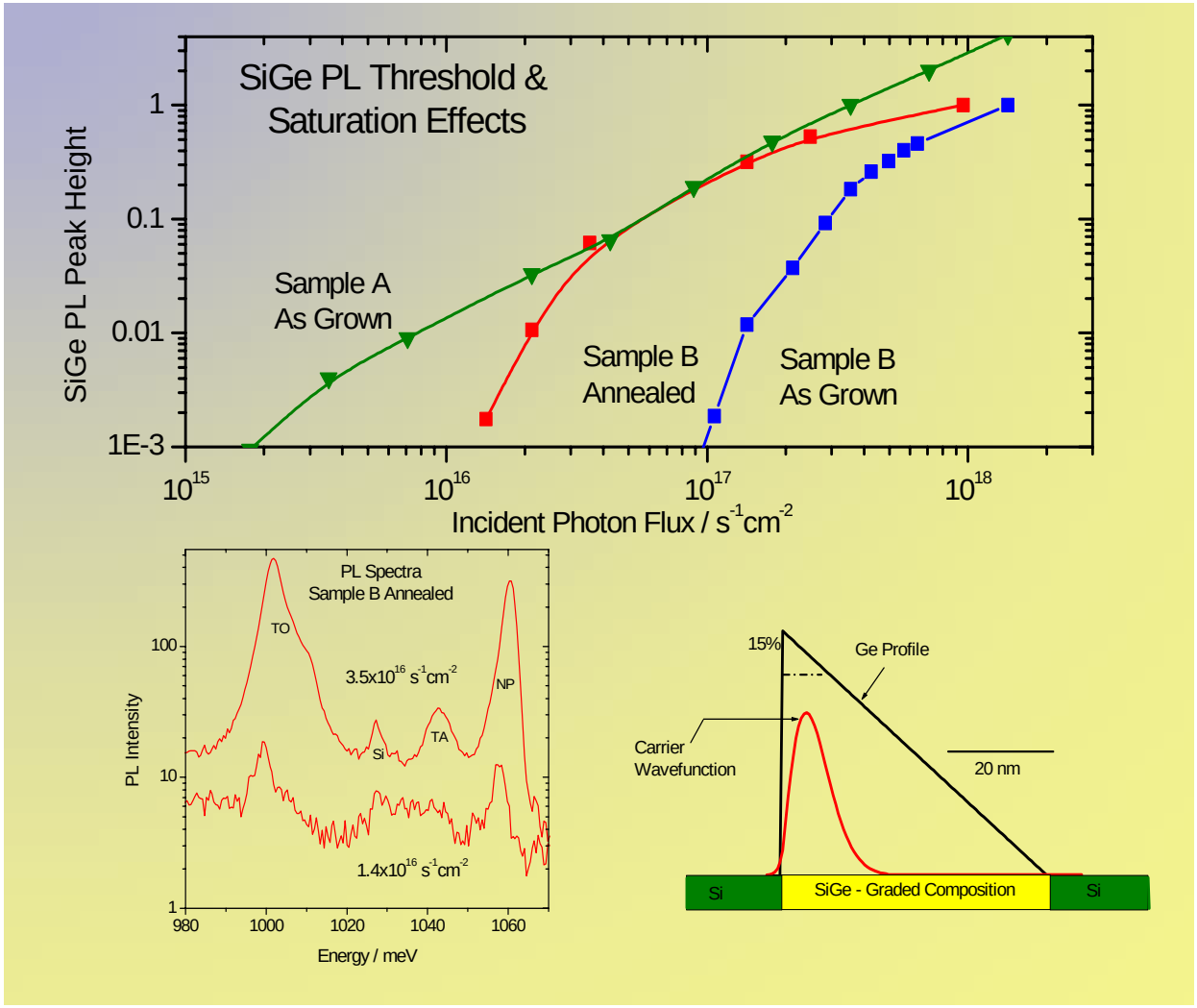
Fourier transform low temperature photoluminescence apparatus.



PL spectra from SiGe HBT transistors

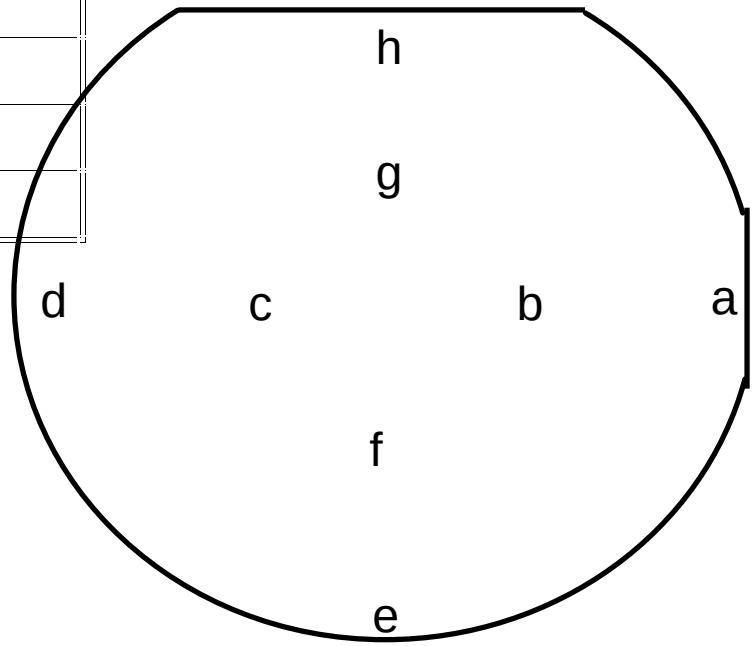


PL of SiGe HBT

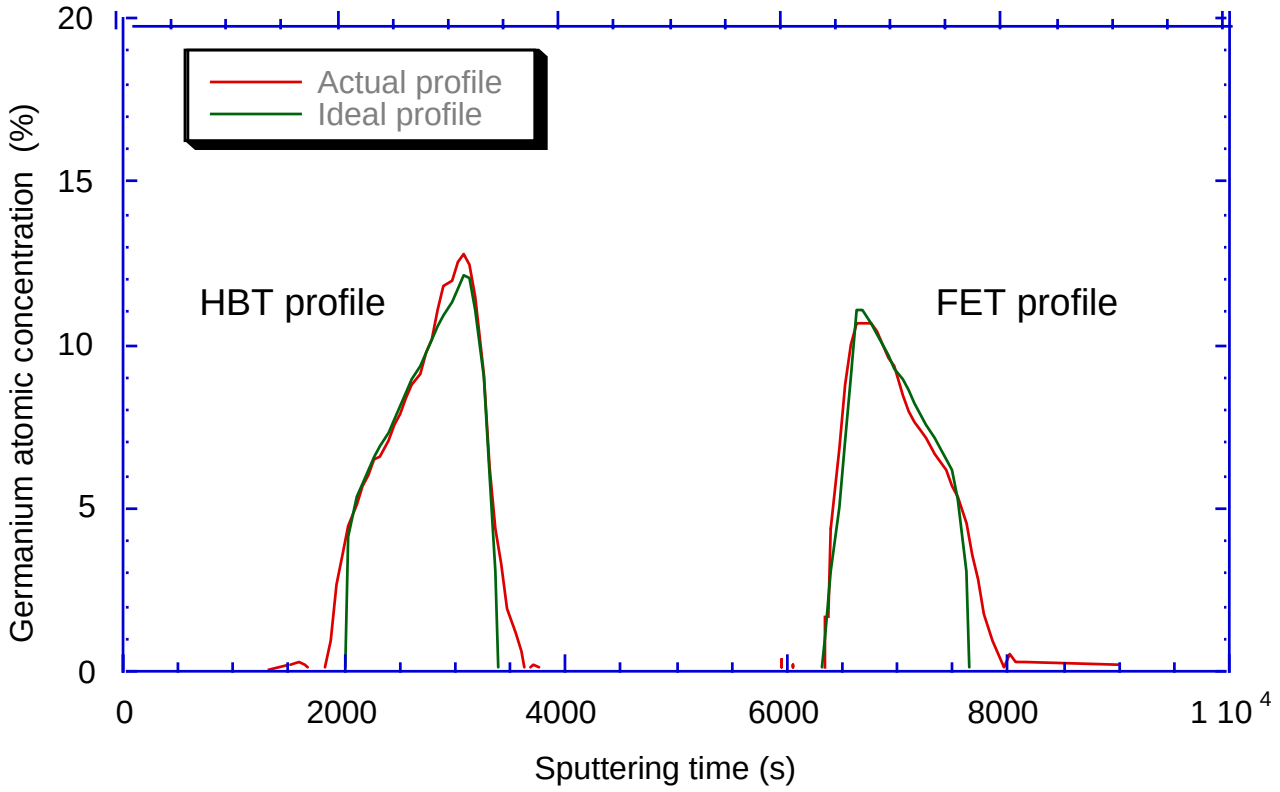


Photoluminescence Mapping of Composition and Bandgap on a 6" wafer

Sample point	"NP" energy (meV)	Energy bandgap (meV)	Composition (% of Ge)
a	1080	1092.2	8.97
b	1082.5	1094.7	8.69
c	1085.2	1097.4	8.39
d	1083.3	1095.5	8.60
e	1082.5	1094.7	8.69
f	1084.8	1097.0	8.44
g	1083.7	1095.9	8.56
h	1079	1091.2	9.08



Auger Electron Spectroscopy
Of Graded germanium concentration profiles



Trends in “novel” epitaxy in Si based materials

For graded SiGe buffers
- Low CoO, defect density reduction, flatness

Thin SiGe epitaxy with defect nucleation layer
- SOI substrates

Lower thermal budget in CMOS
- low leak rate tools
- new precursors with high GR at <600C, e.g.trisilane

Selectivity, patterned wafers, SOI substrates

High mobility channels
- Pure Ge, III-V’s on Ge on SiGe, epitaxial metals