Physics of Advanced CMOS VLSI

Dennis Buss
Texas Instruments, Inc.
Dallas, Texas USA

Conclusions

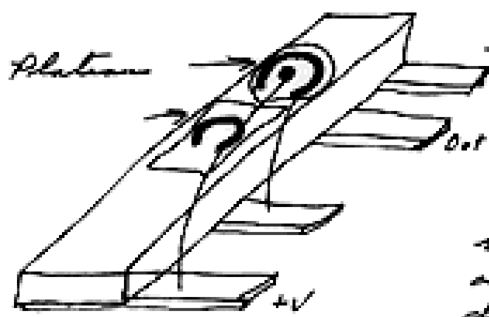
- For the past 35 years, transistors have been developed using “Electrical Engineering Physics”, which was codified in the early 60’s
- As the industry approaches the “End of Roadmap”, Electrical Engineering Physics is no longer sufficient. Technology development increasingly requires
  - Sophisticated quantum physics
  - Non-equilibrium Boltzmann transport
  - Material science at the atomic and electron orbital level
- This has implications for
  - Physics education
  - Career opportunities for physicists in the semiconductor industry

Agenda

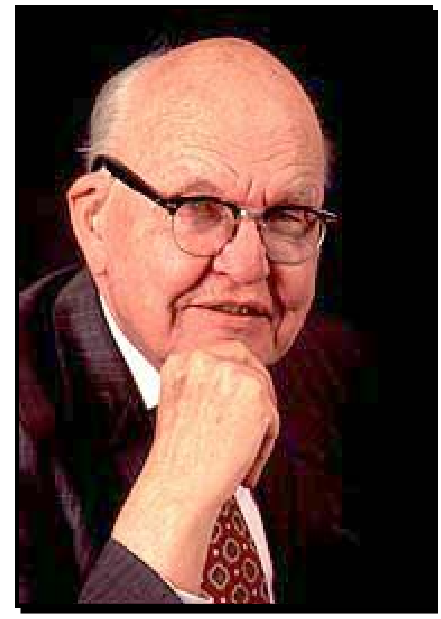
- Introduction to CMOS VLSI Technology
- Physics challenges to continued VLSI scaling
- Conclusion

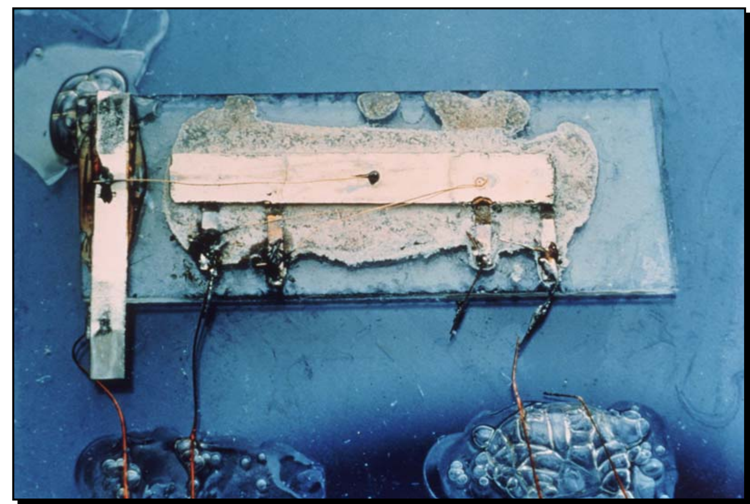
Integrated Circuit – 1958

20
EO NO. 043601
DATE Sept 12, 1958



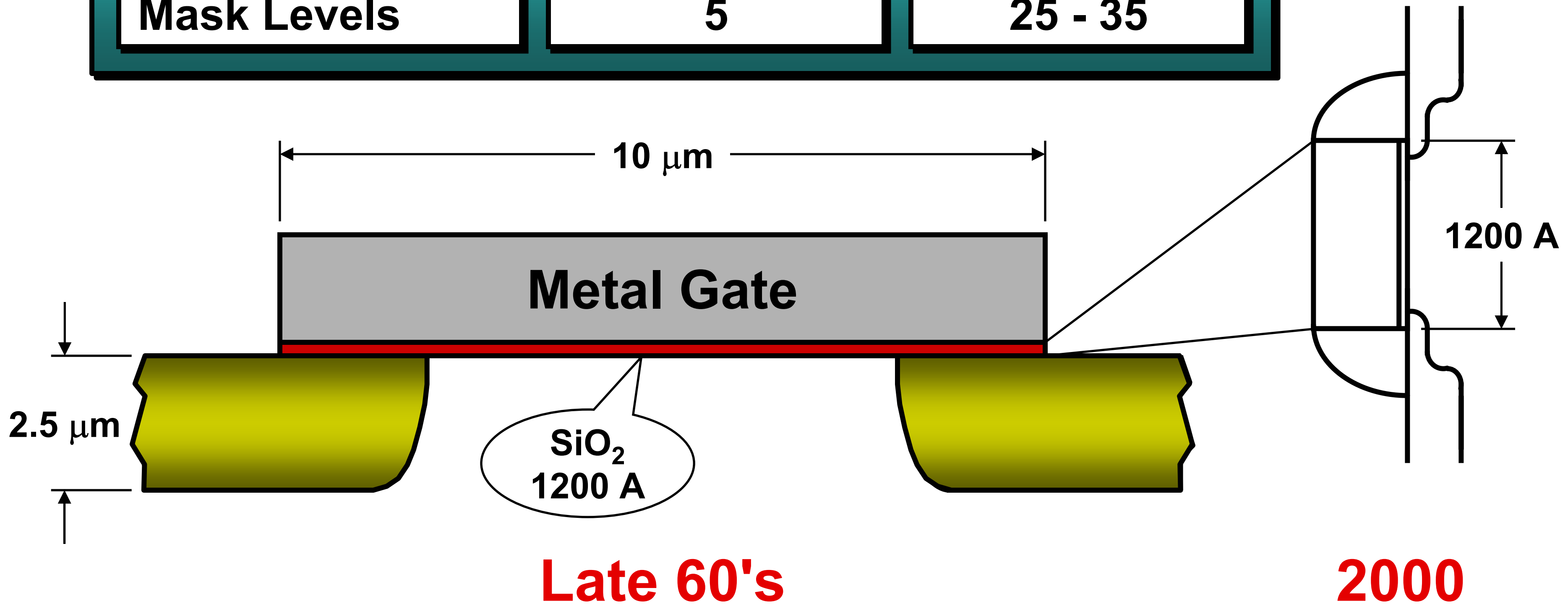
US Patent # 3,138,743
Filed Feb. 6, 1959



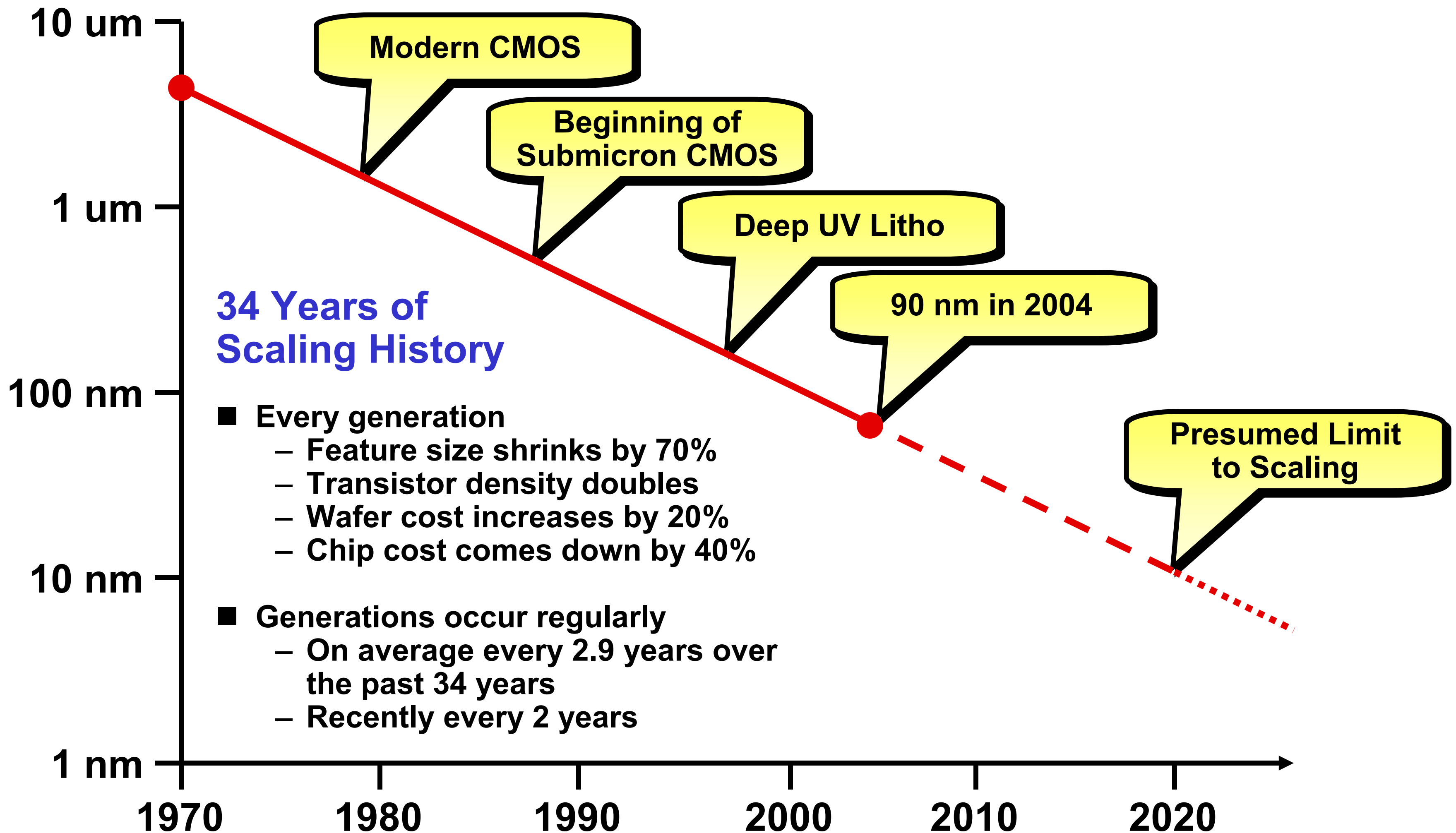


MOS Scaling

	Late 60's	2000
Gate Length	10 μm	120 nm
Oxide Thickness	120 nm	12 A
Gate Material	Al	poly-Si
Junction Depth	2.5 μm	25/70 nm
Interconnect	Al	Cu
Mask Levels	5	25 - 35



Moore's Law

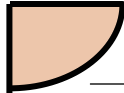


34 Years of History

	1970	Today	Change
Feature Size	6 um	90 nm	70x Reduction
Transistor Density			5000x Increase
Chip Size	~10 mm^2	~400 mm^2	40x Increase
Transistors/Chip	1000	200 M	200,000x Increase
Clock Frequency	100 kHz	> 1 GHz	>10,000x Increase
Power Dissipation	~100 mW	~100 W	~1000x Increase
Fab Cost	~$10 M	>$1 B	>100x Increase
WW IC Revenue	$700 M	$170 B	240x Increase
WW Electronics Revenue	$70 B	$1.1 T	16x Increase

Electrical Engineering Physics

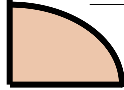
Electron Mass



Conduction Band

E_g

Hole Mass



Valence Band

$$f(E) = \frac{1}{e^{(E - E_F)/kT} + 1}$$

$$n = N_c e^{-(E_c - F_n)/kT}$$

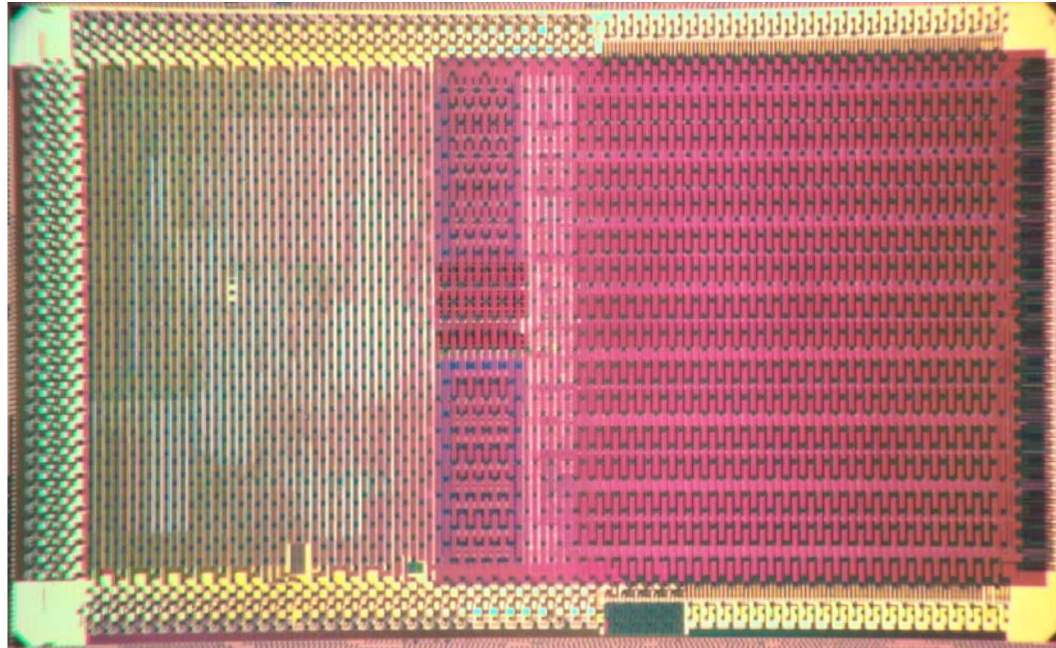
$$p = N_v e^{-(F_p - E_v)/kT}$$

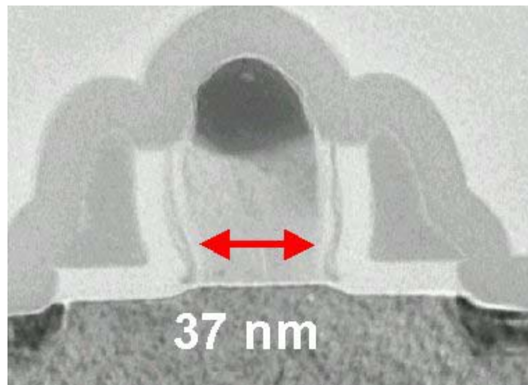
$$\frac{d^2V(x)}{dx^2} = \frac{\rho(x)}{\varepsilon} = \frac{q}{\varepsilon}(p - n + N_d^+ - N_a^-)$$

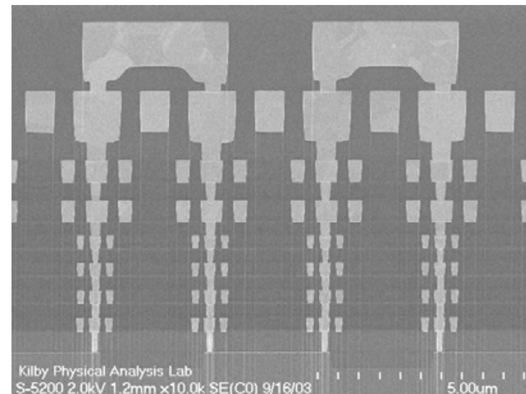
$$J_n(x) = q\mu_n n(x)\varepsilon(x) + qD_n \frac{dn(x)}{dx}$$

$$J_p(x) = q\mu_p p(x)\varepsilon(x) - qD_p \frac{dp(x)}{dx}$$

High Performance Processor @ 90nm

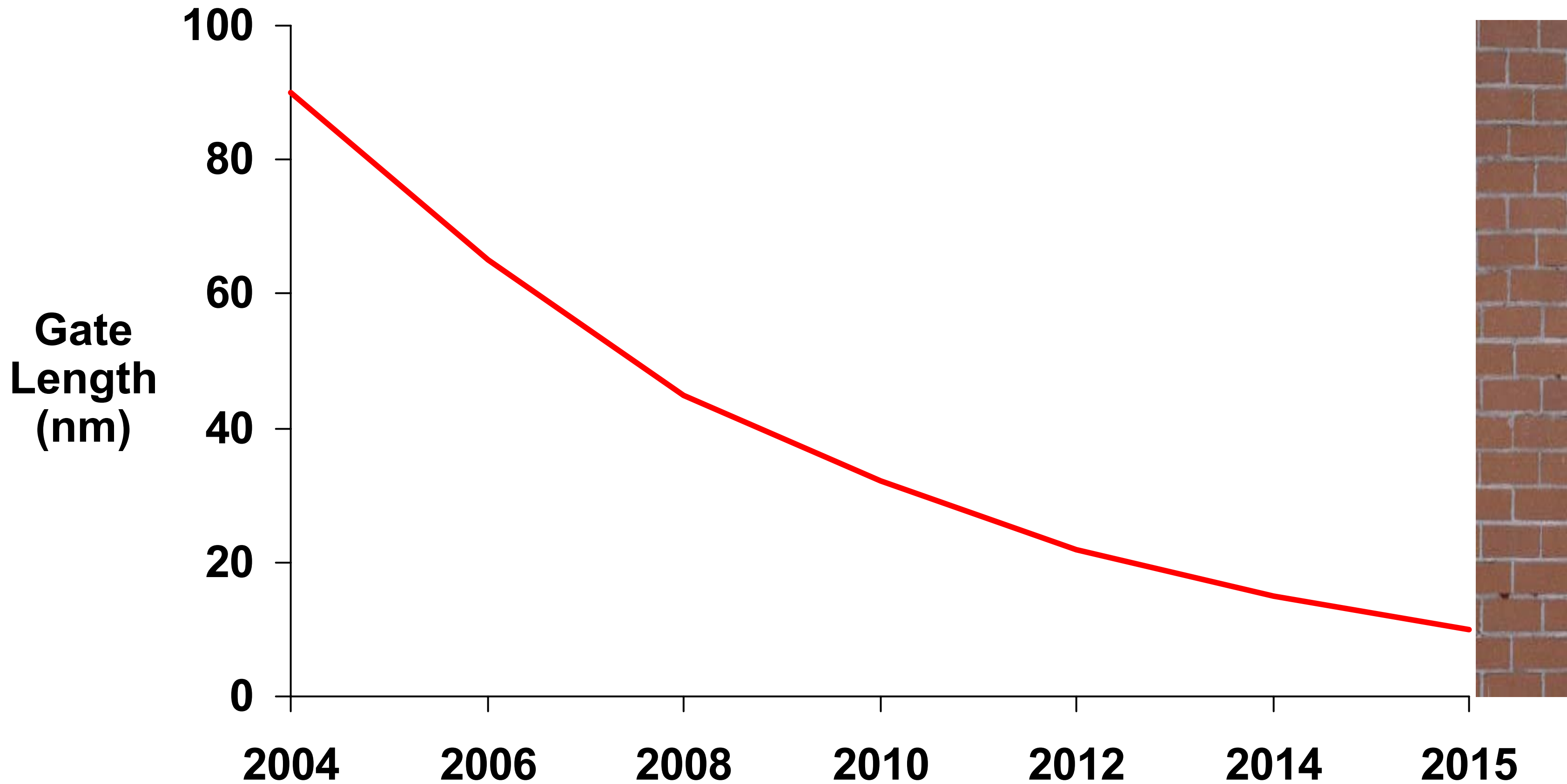




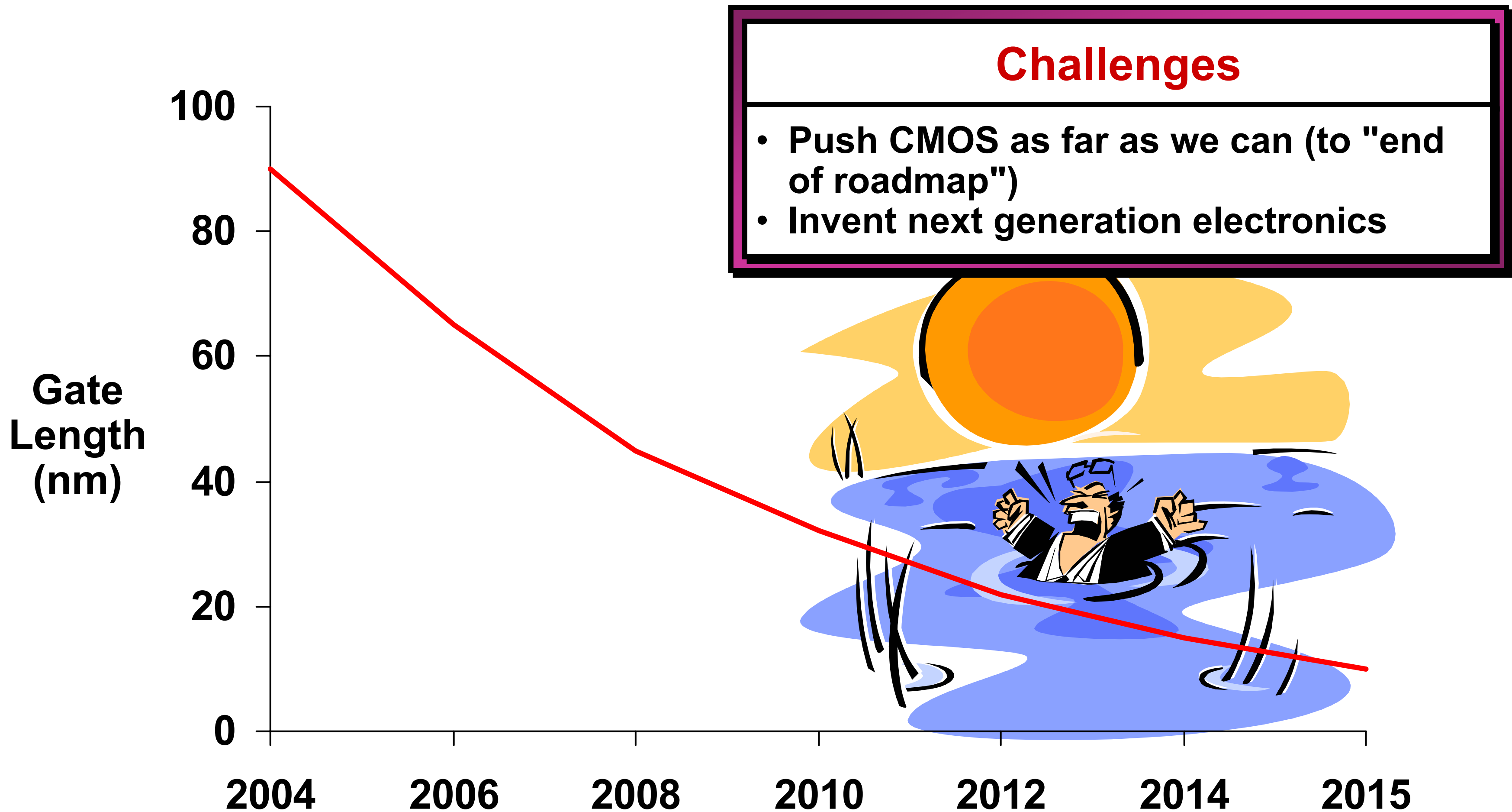


- 256 million transistors
- 37nm gate length
- PNO gate: 10 nm EOT
- $NiSi_2$/Poly gate
- 8 levels Cu with low-k interlevel dielectric

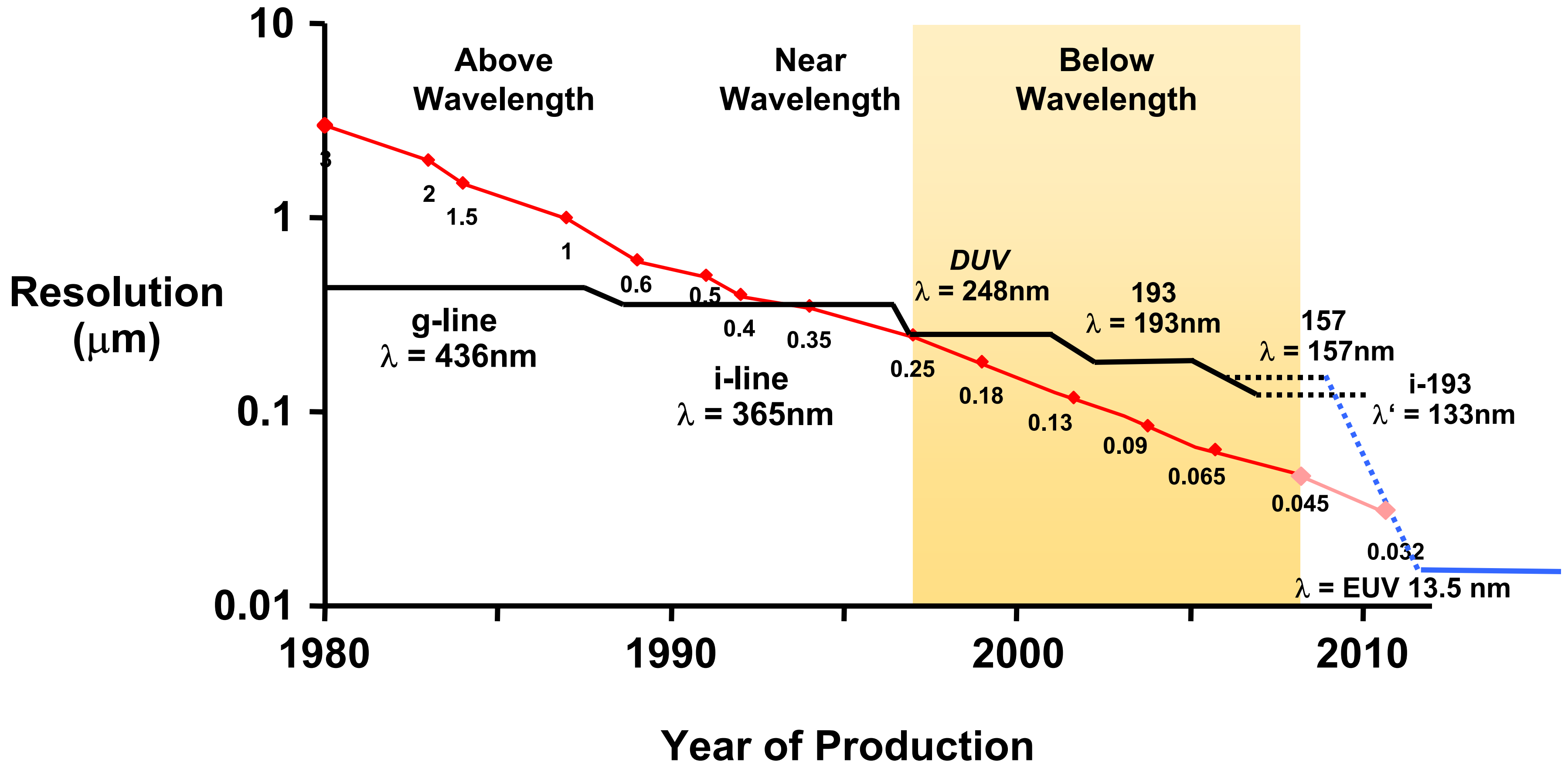
Heading for Change



Heading for Change



Lithography



Lithography will not ultimately limit IC feature size!

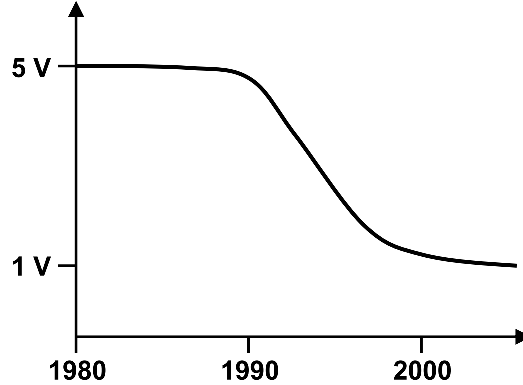
Agenda

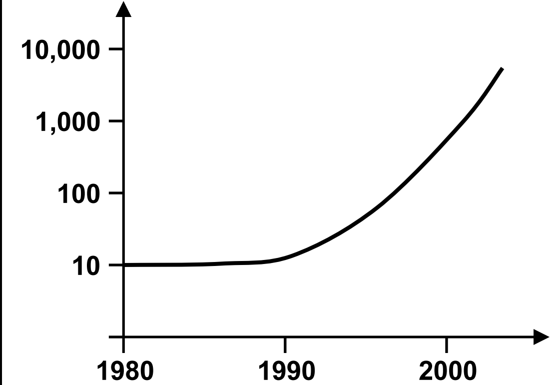
- Introduction to CMOS VLSI Technology
- Physics Challenges to Continued VLSI Scaling
  - Gate insulator
  - Gate electrode
  - Carrier scattering
  - Quantum behavior of carriers in the presence of stress
  - Non-equilibrium Boltzmann transport
  - Tunneling
  - Discrete positioning of dopant atoms
  - Electrostatics
  - Simulation
- Conclusion

Gate Insulator

Delay ~ $\frac{CV}{I_{drive}}$

Power $\approx 1/2\ CV^2F_c$

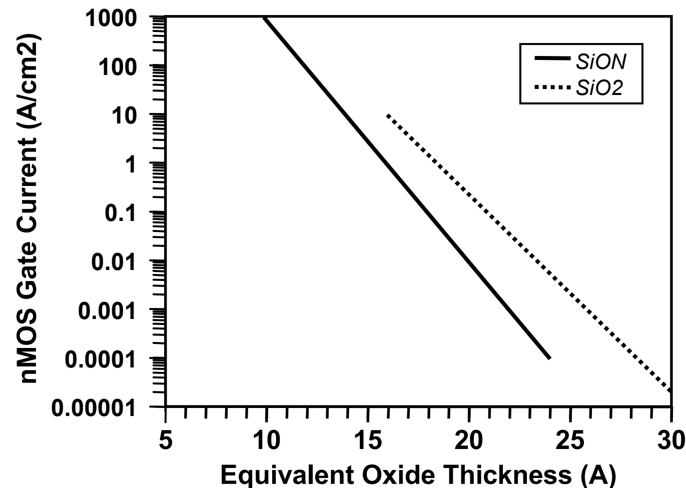




Inversion Layer Charge

$$Q_{inv} \approx D_{ox} = \varepsilon_{ox}E_{ox}$$

$$\approx \varepsilon_{ox} \frac{V_{dd}}{t_{ox}}$$

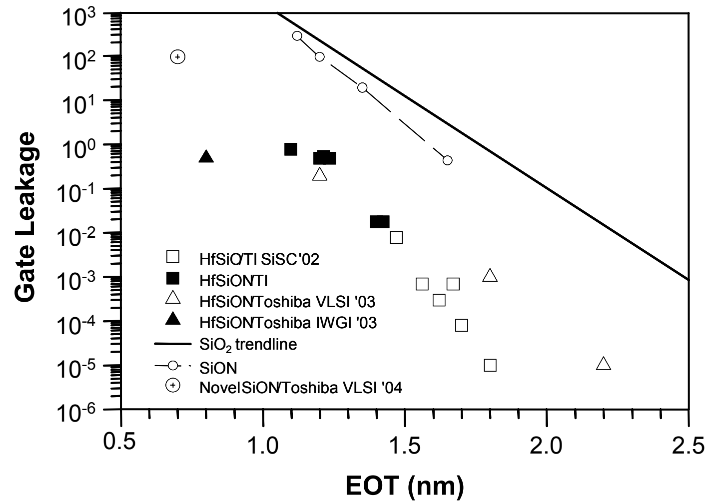


Voltage Reduction Achieved by

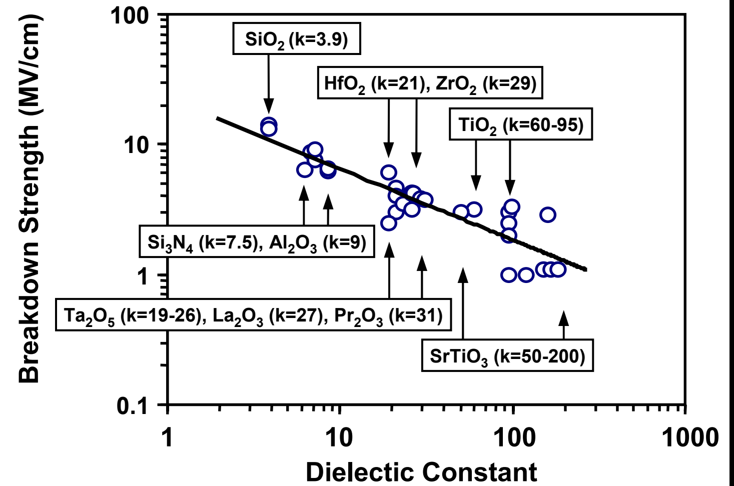
- Reduction in $t_{ox} \approx$ 10A in 2004
- Increase in ε_{ox} using Plasma Nitrided Oxide (PNO)

Gate Insulator

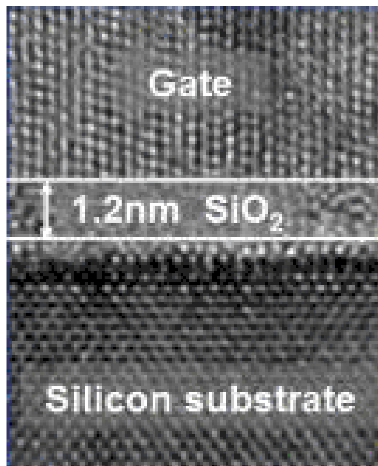
Good News

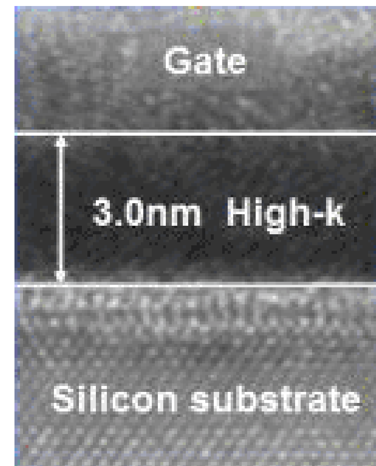


Bad News

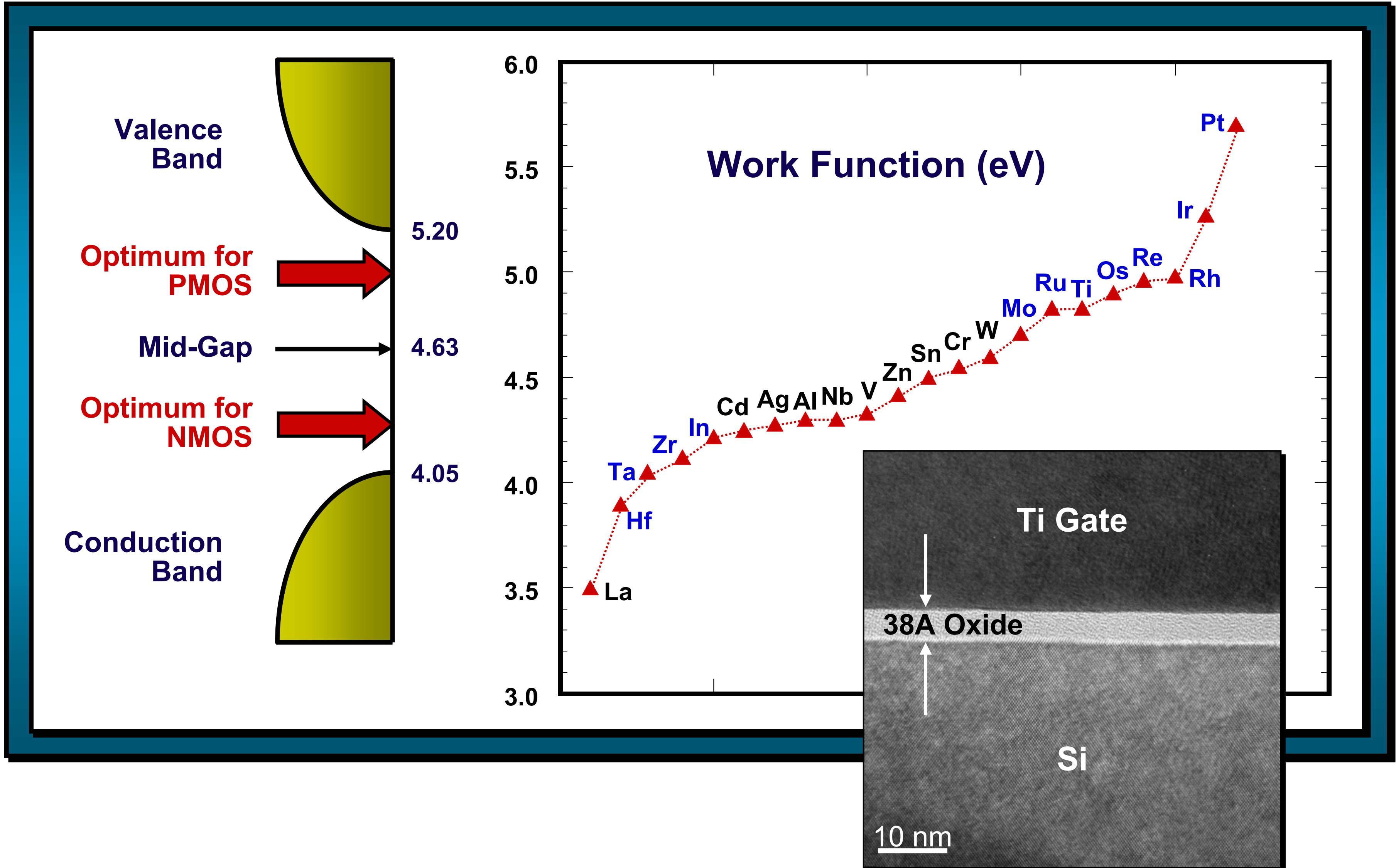


Hi-k also degrades channel mobility



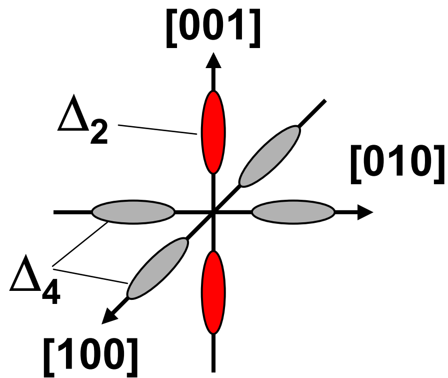


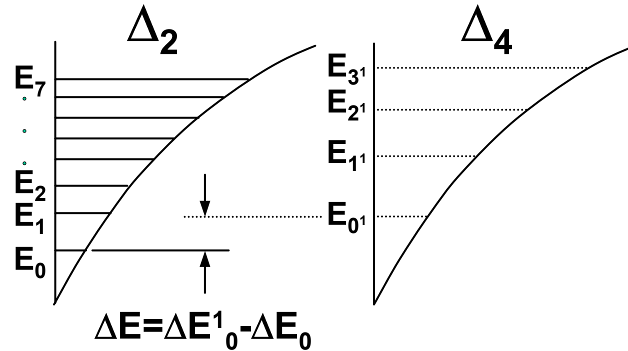
Metal Gate



Electrons in Si

Stark Effect





Modern CMOS

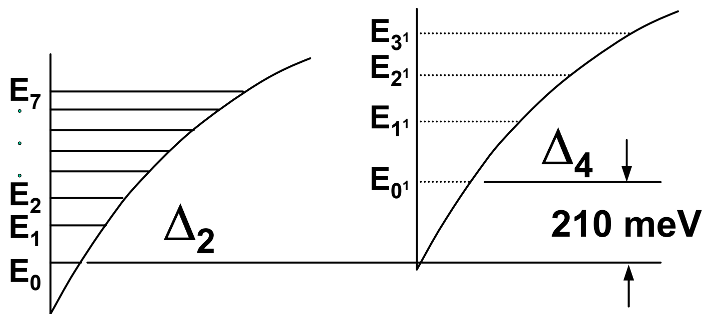
Vertical Field E ≈ 1.2 MV/cm

Stark Quantization results in

$\Delta E \approx 75$ meV

$\Delta V_t \approx 50$ mV

Effect of Strain



Bi-axial tensile strain of 1.3 GPa results in

$\Delta E_{strain} \approx 135$ meV

Mobility increase ≈ 80%

I_{drive} increase ≈ 20%

Holes in [110] Uniaxially Compressed Si

Si

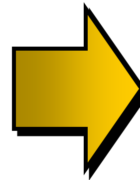
[110]

k_y

$| p_x,p_y>$

k_x

Unstrained Heavy Hole (HH)



LH,HH

HH_S

LH_S

Mobility Degrades

Mobility Improves

k_y

$| s,p_x,p_y ,p_z>$

k_x

Strained Heavy Hole (HHS)

Discrete Channel Dopants

W = 40nm

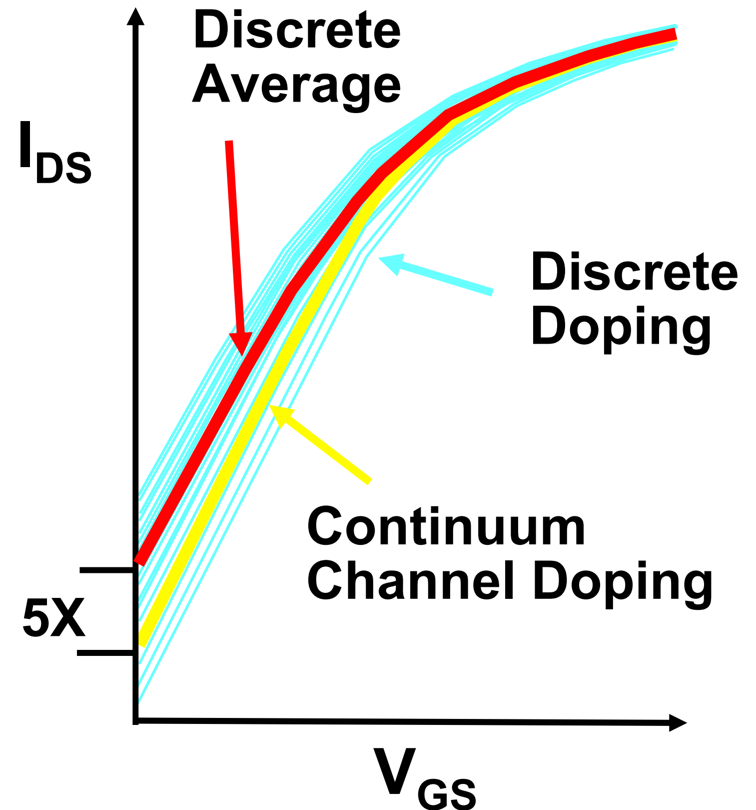
E_C

L = 20nm

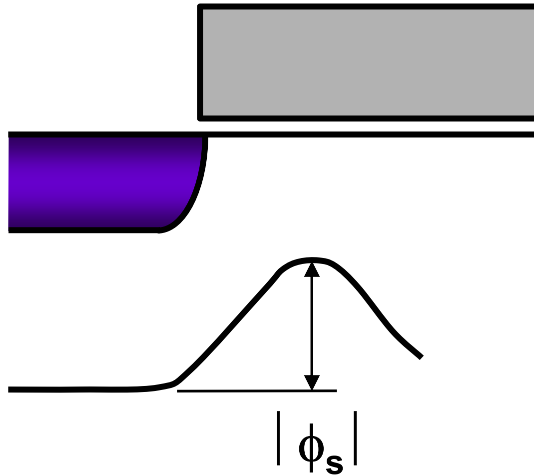
Current Density

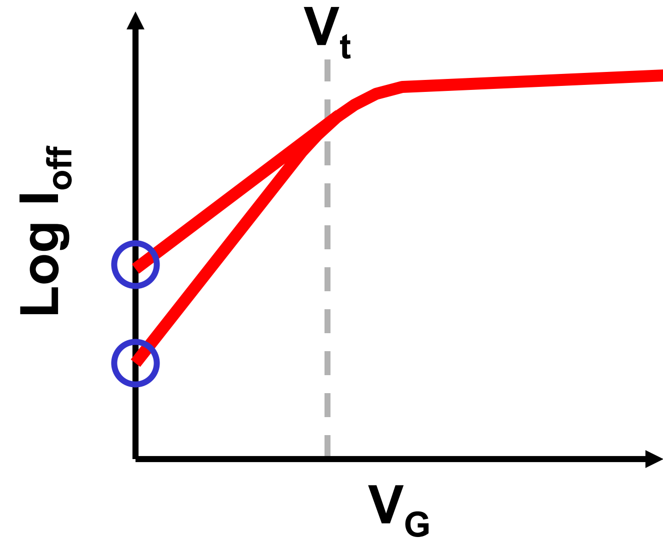
Off-Current Filament

Discrete Channel Dopants Introduce I_{OFF} Fluctuations and I_{OFF} Degradation



Myth of the MOSFET Switch





In the Off State

$$I_D \sim e^{\frac{-q|\phi_s|}{kT}}$$

$$\frac{\Delta \log I_D}{\Delta V_G} = \frac{q}{kT}\ \underbrace{\frac{C_{ox} + C_P}{C_{ox}}}_{\frac{\partial|\phi_s|}{\partial V_G}}\ \log_{10} e$$

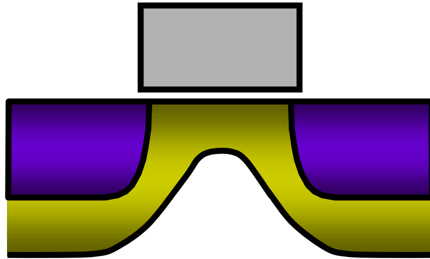
Sub-Threshold Slope
60 - 100 mV/decade

For V_t = 300mV ⇨ 5 - 3 decades

$I_{on} \approx$ 1 mA/um

$I_{off} \approx$ 10 nA/um - 1 uA/um

Electrostatics



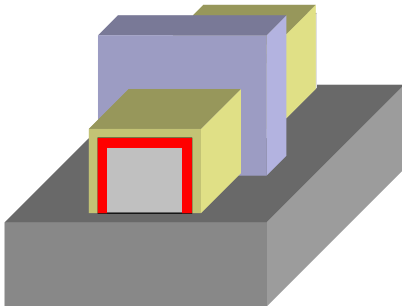
Critical Scaling Parameters

L W

t_{ox} x_{jun} x_{dep}

t_{ox} and x_{dep} are encountering scaling limits. This results in ...

- Degraded sub-threshold slope $\frac{kT}{q} \frac{C_{ox} + C_P}{C_{ox}}$
- Increased drain induced barrier lowering (DIBL)



Multi-Gate FETs show promise of extending scaling for several generations beyond planar CMOS

Conclusion

- **Scaling CMOS to the "End of Roadmap" will require sophisticated condensed matter physics.**
  - **Gate stack: Atomic and electron orbital understanding of this complex material system**
  - **Quantum behavior of carriers**
    - **High perpendicular E field**
    - **Stress**
  - **Non-equilibrium Boltzmann transport**
  - **Tunneling: Gate insulator and Drain-to-Substrate**
  - **Simulation**

- **Sophisticated condensed matter physics will also be required to invent and develop electronics beyond CMOS**
  - **Single Electron Transistor (SET)**
  - **Carbon Nano-tube (CNT)**
  - **Molecular Electronics**
  - **Spintronics**
  - **Quantum Computing**