SiGe(C) MOSFET Technology

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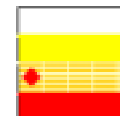
- Issues in Scaled CMOS
- Bandstructure, Transport and Strain
- Enhanced Mobility Channels
  - Strained Si and SiGe(C)
- Multi-Gate and Novel MOSFETs
- Process Integration Challenges

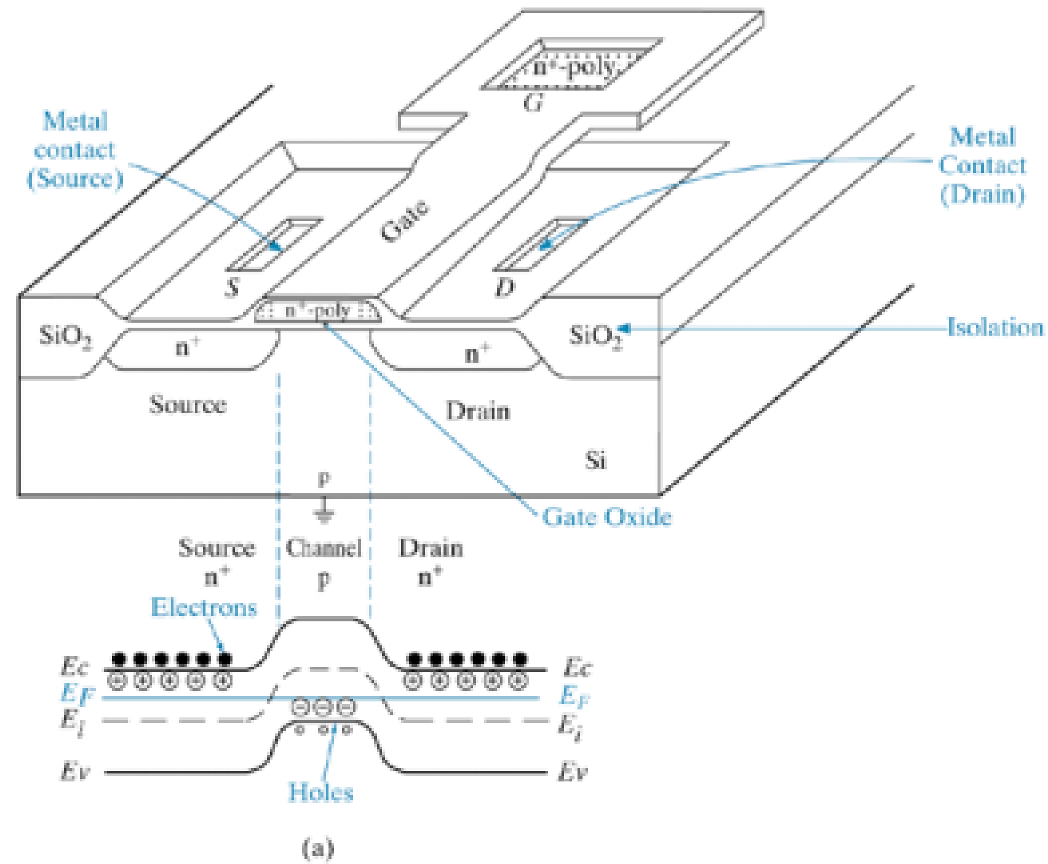
ITRS, 2003

Table 47b High-performance Logic Technology Requirements—Long-term

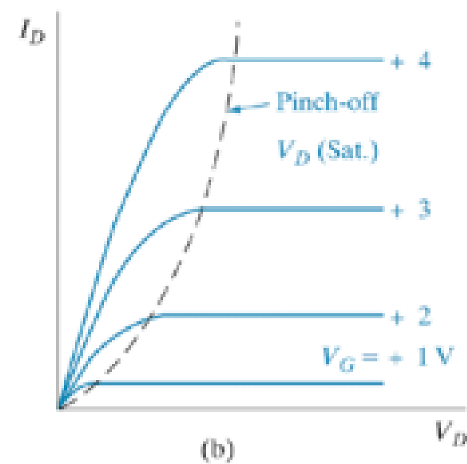
Year of Production	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM ½ Pitch (nm)	45	35	32	25	22	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	42	38	30	27	21
MPU/ASIC ½ Pitch (nm)	45	35	32	25	22	18
MPU Printed Gate Length (nm)	25	20	18	14	13	10
MPU Physical Gate Length (nm)	18	14	13	10	9	7
Physical gate length high-performance (HP) (nm) [1]	18	14	13	10	9	7
EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7	0.7	0.6	0.6	0.5	0.5
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	1.1	1.1	1.0	1.0	0.9	0.9
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	1.9E+03	2.4E+03	7.7E+03	1.0E+04	1.9E+04	2.4E+04
Nominal power supply voltage (V_{dd}) (V) [6]	1.0	0.9	0.9	0.8	0.8	0.7
Saturation threshold voltage (V) [7]	0.15	0.14	0.11	0.12	0.10	0.11
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (mA/µm) [8]	0.1	0.1	0.3	0.3	0.5	0.5
Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (mA/µm) [9]	1900	1790	2050	2110	2400	2190
Required "mobility/transconductance improvement" factor [10]	2.0	2.0	2.0	2.0	2.0	2.0
Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]	0.6	0.5	0.5	0.5	0.5	0.5
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.1	1.1	1.1	1.3	1.3	1.3
Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	135	116	107	88	79	60
Ideal NMOS device gate capacitance (F/µm) [14]	5.65E-16	4.39E-16	4.49E-16	3.45E-16	3.45E-16	2.69E-16
Parasitic fringe/overlap capacitance (F/µm) [15]	1.80E-16	1.50E-16	1.40E-16	1.20E-16	1.00E-16	8.00E-17
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.39	0.30	0.26	0.18	0.15	0.11
Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.06	4.05	4.64	6.80	8.08	10.77
Nominal logic gate delay (NAND gate) (ps) [18]	9.88	7.47	6.52	4.45	3.74	2.81
NMOSFET power-delay product (J/µm) [19]	7.45E-16	4.77E-16	4.77E-16	2.98E-16	2.85E-16	1.71E-16
NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	1.10E-06	9.90E-07	2.97E-06	2.64E-06	4.40E-06	3.85E-06

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



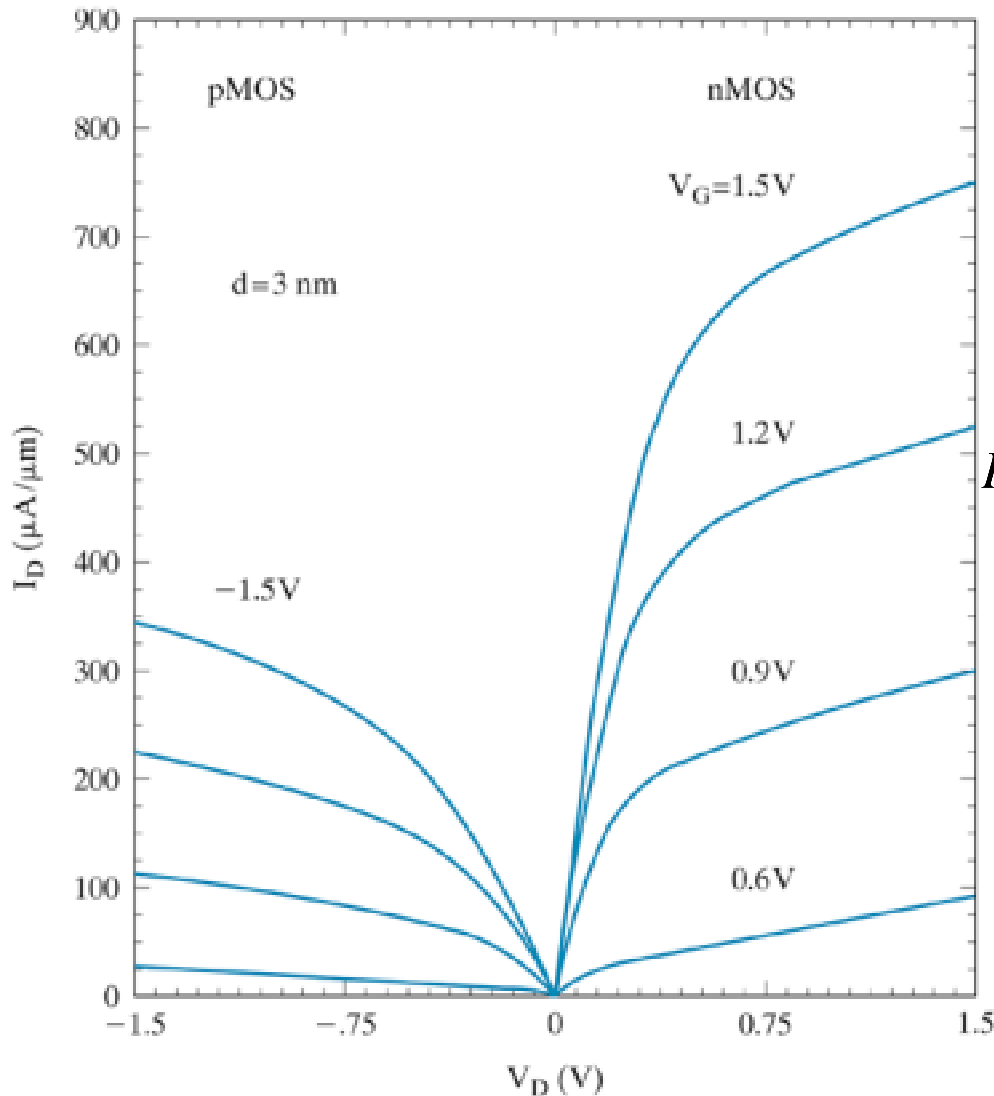


(a)



(b)

Streetman and Banerjee, *Solid State Electronic Devices*, Prentice Hall



For LONG channel

$$I_D = \frac{W}{L}\mu C_{0X}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^{\ 2}\right]$$

$$I_{DSAT} = \frac{W}{L}\mu C_{0X}\left[(V_G - V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^{\ 2}\right]$$

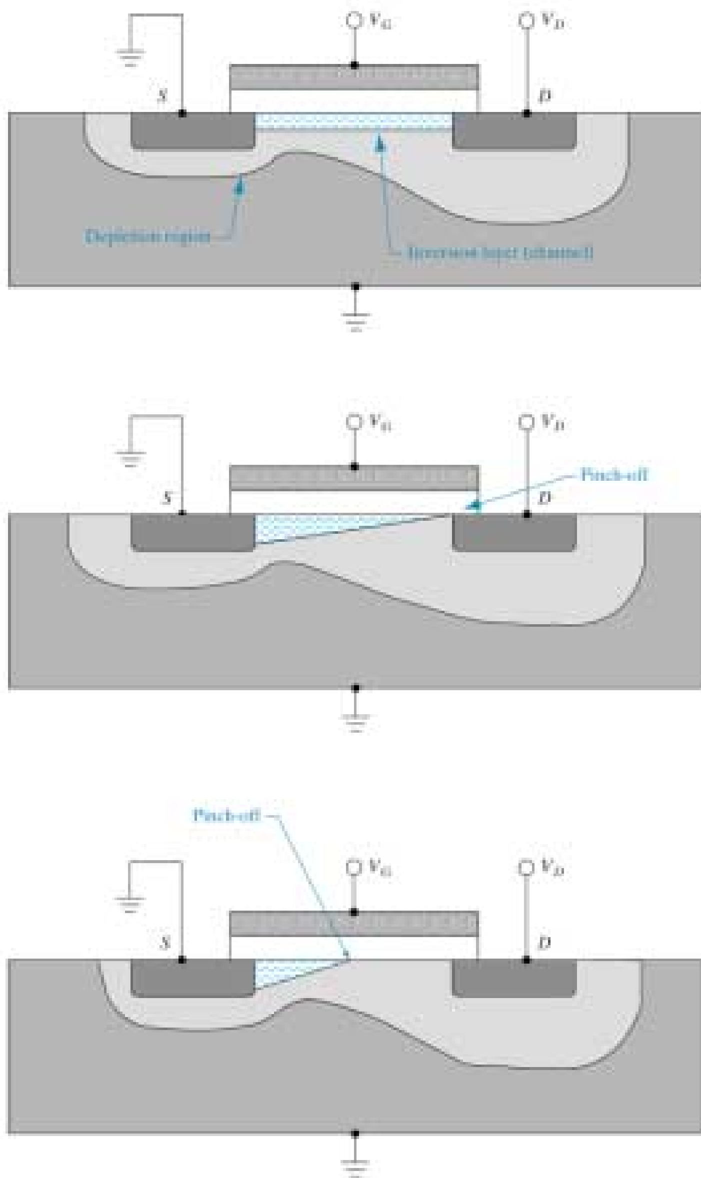
$$where[V_{DSAT} = (V_G - V_T)]$$

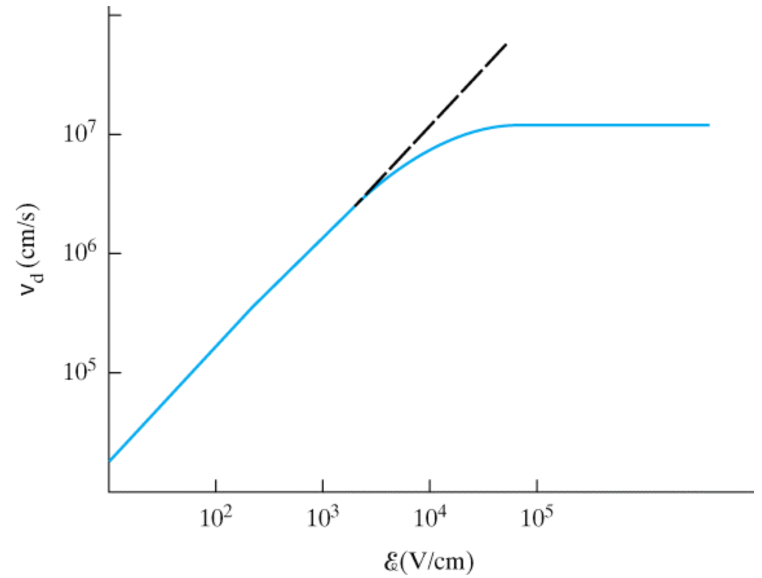
$$I_{DSAT} = \frac{W}{L}\mu C_{0X}\left[\frac{1}{2}V_{DSAT}^{\ 2}\right]$$

For SHORT channel,

$$I_D \approx WC_{OX}(V_G - V_T)\,\mathrm{v_{sat}}$$

Experimental output characteristics of n-channel and p-channel MOSFETs with 0.1 micron channel lengths. The curves exhibit almost equal spacing, indicating a linear dependence of I_D on V_G, rather than a quadratic dependence. We also see that I_D is not constant but increases somewhat with V_D in the saturation region. The p-channel devices have lower currents because hole mobilities are lower than electron mobilities.





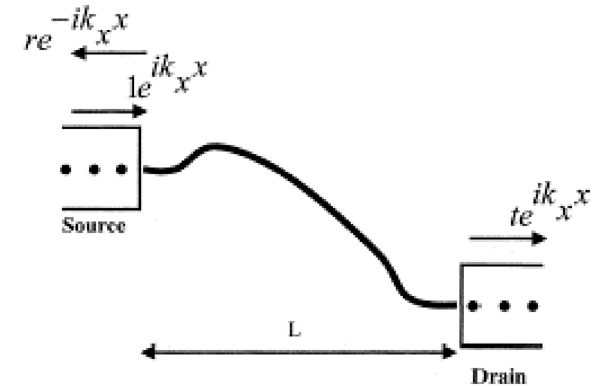
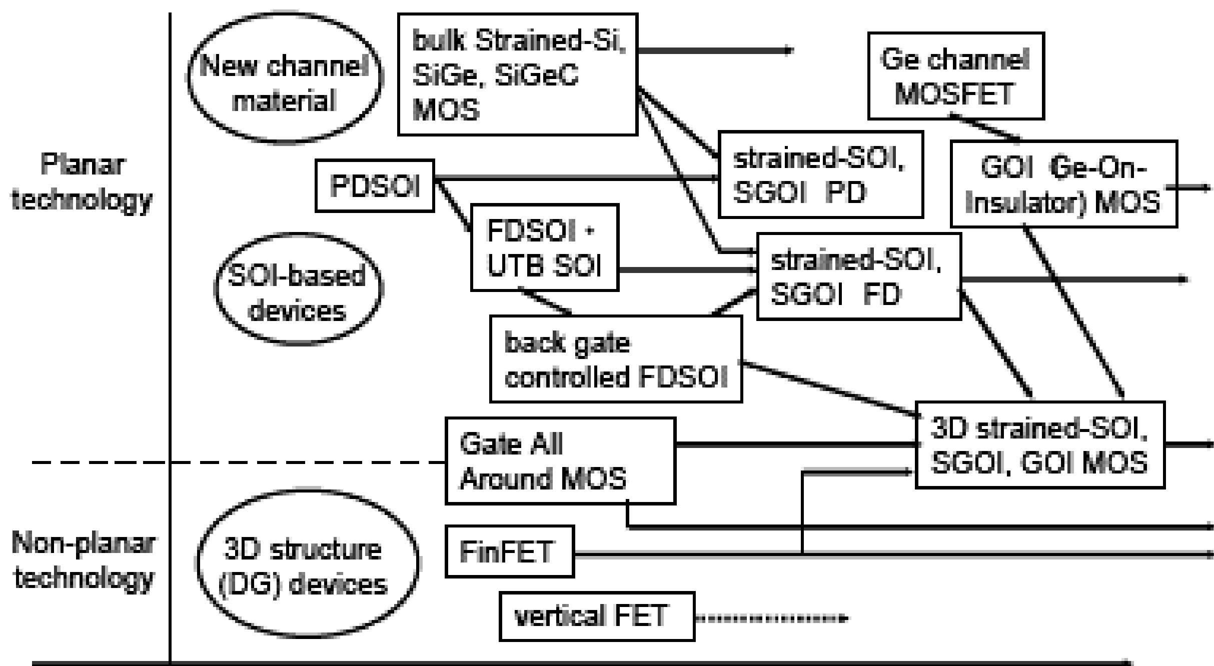


Fig. 2. Sketch of the generic subband energy versus position along the channel (x). Also shown are the semi-infinite source-drain contacts (bounded by open rectangles) and the boundary conditions for injection of a unit amplitude from the source end. The nodes within the device are numbered 1 to N and the active device extends from $x = 0$ (source) to $x = L$ (drain).

$$I_{DSAT} = [C_O W v_T]\left(\frac{1-r_c}{1+r_c}\right)(V_G - V_T)$$

For short "quasi-ballistic" MOSFETs, current is limited by source-to-channel injection of thermal carriers. Since, here the longitudinal field is low, ***this injection is limited by low field mobility.*** (Natori and Lundstrom)



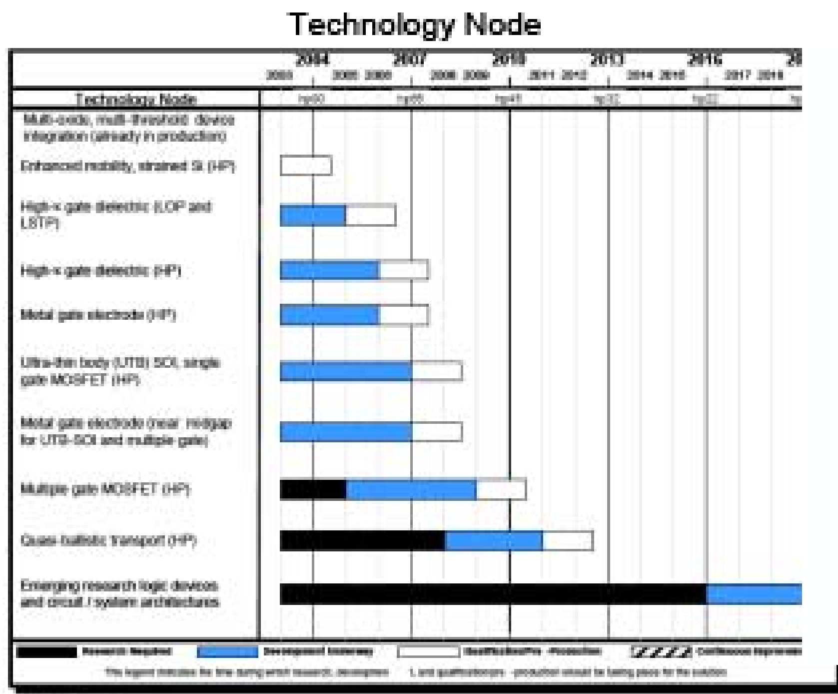
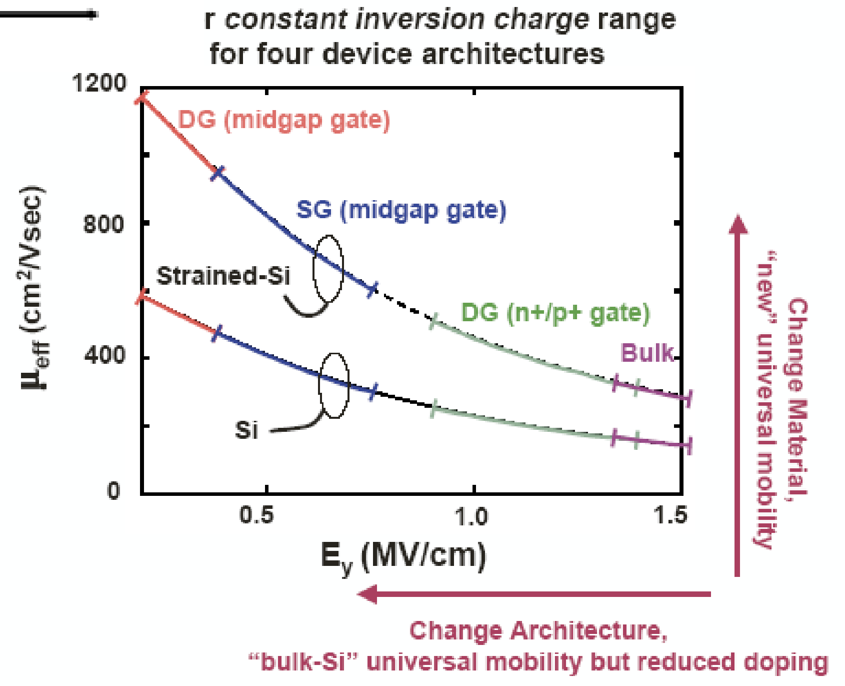


Figure 26 Logic Potential Solutions

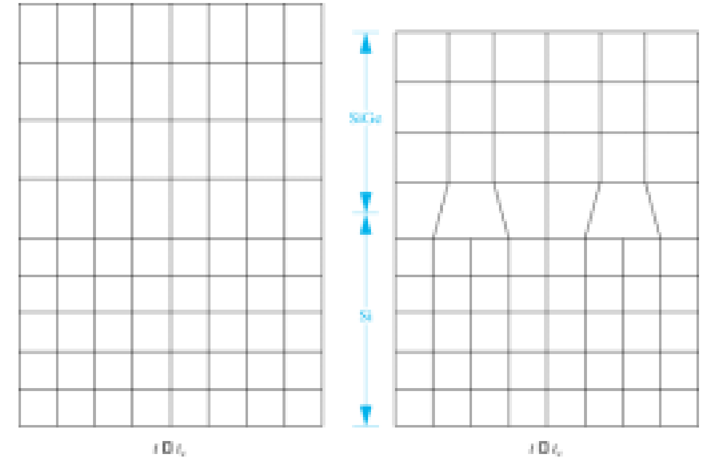


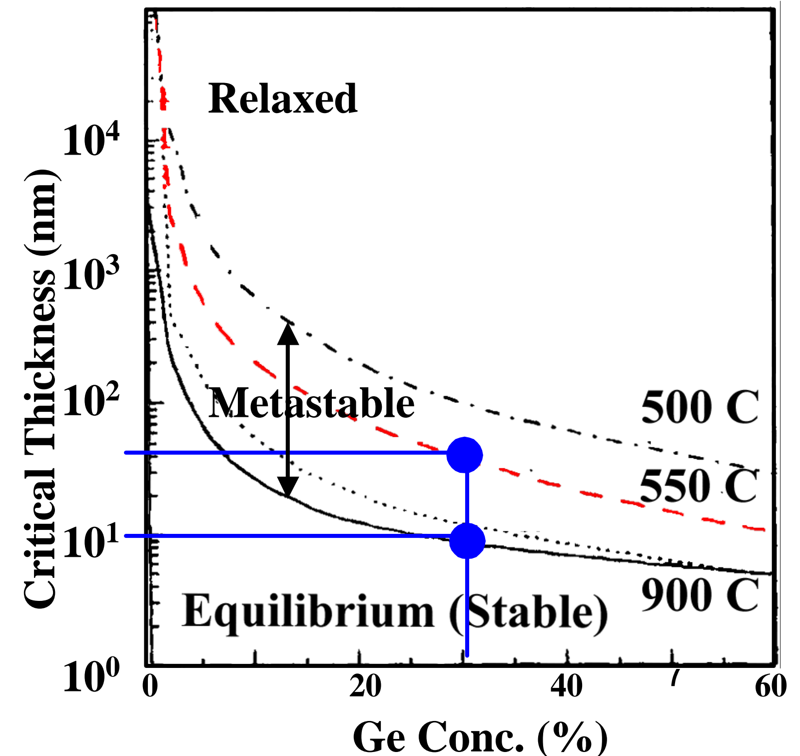
Compressive Strain in $Si_{1-x}Ge_x$

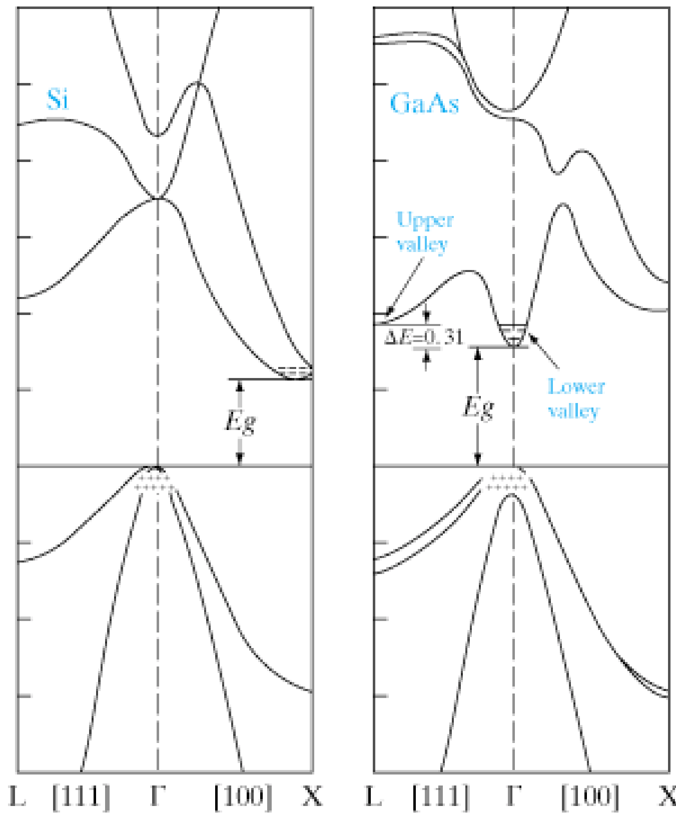
- $Si_{1-x}Ge_x$ Bulk Properties.
  - 0 to 100% Ge possible
  - Lattice constant and bandgap given by Vegard's Law:

$$a_{SiGe}(x) = a_{Si}(1-x) + a_{Ge}(x)$$

- $Si_{1-x}Ge_x$ on Si
  - Up to 4.2% lattice mismatch
  - Strained epitaxial layers
  - Tetragonal distortion breaks degeneracy in the bandstructure.

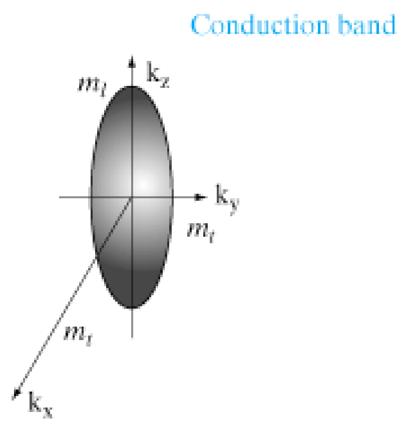






(a)

“Effective mass” $m^* = \frac{\hbar^2}{\left(\frac{d^2E}{dk^2}\right)}$



(b)

$$\mu = \frac{e\langle\tau\rangle}{m^*}$$

$$g_c(E) = 4\pi\left(\frac{m_{de}^*}{h^2}\right)^{\frac{3}{2}}(E - E_c)^{\frac{1}{2}}$$

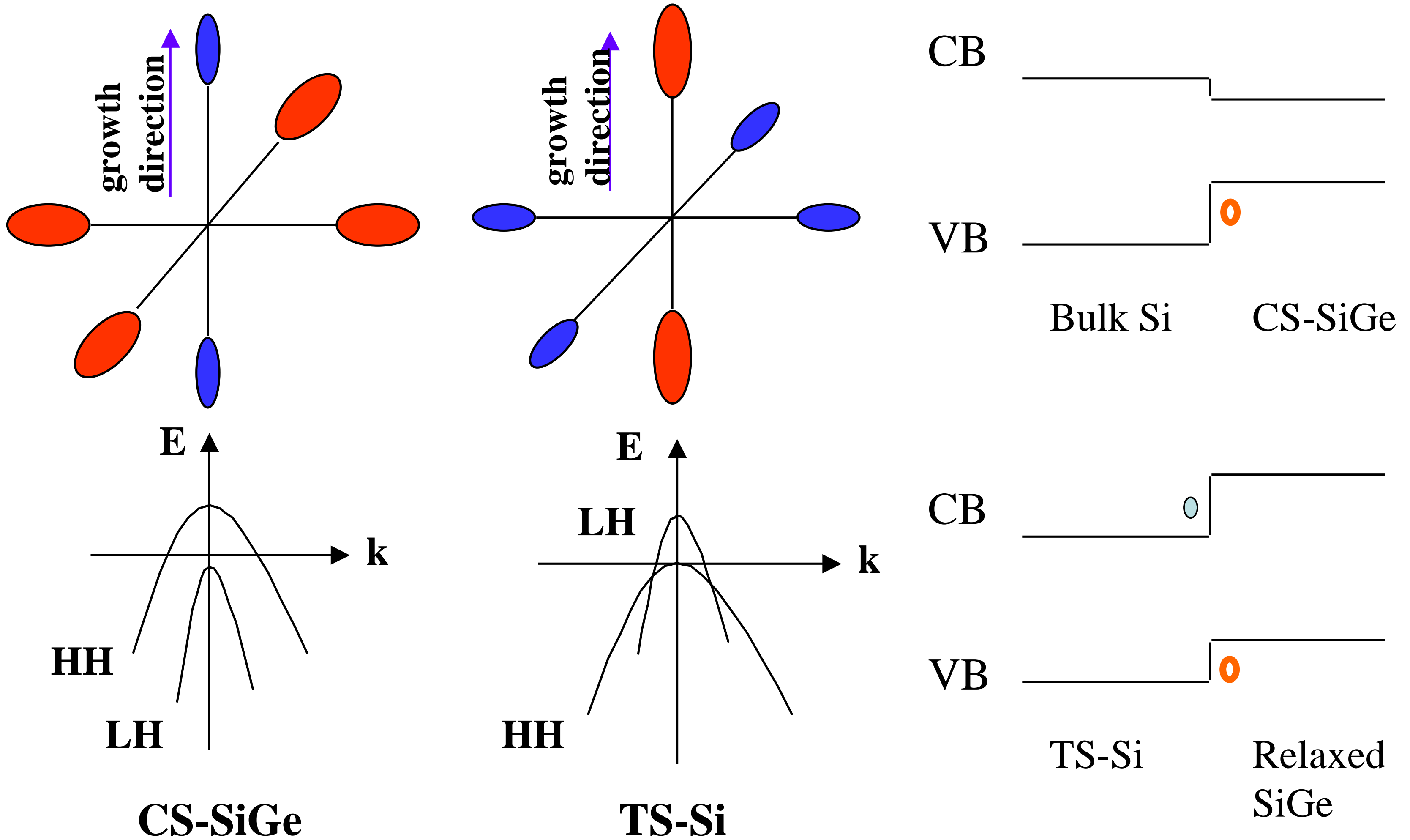
$$m^* = \left(m_1^* m_2^* m_3^*\right)^{\frac{1}{3}}$$

$$m^* = 3\left(\frac{1}{m_1^*} + \frac{1}{m_2^*} + \frac{1}{m_3^*}\right)^{-1}$$

Bandstructure effective mass, m*, is inversely related to curvature of bands, and depends on crystal orientation.
Density of states m* is related to geometric mean of bandstructure m*. Must count number of “equivalent” valleys.

Conductivity m* is harmonic mean of bandstructure m*.

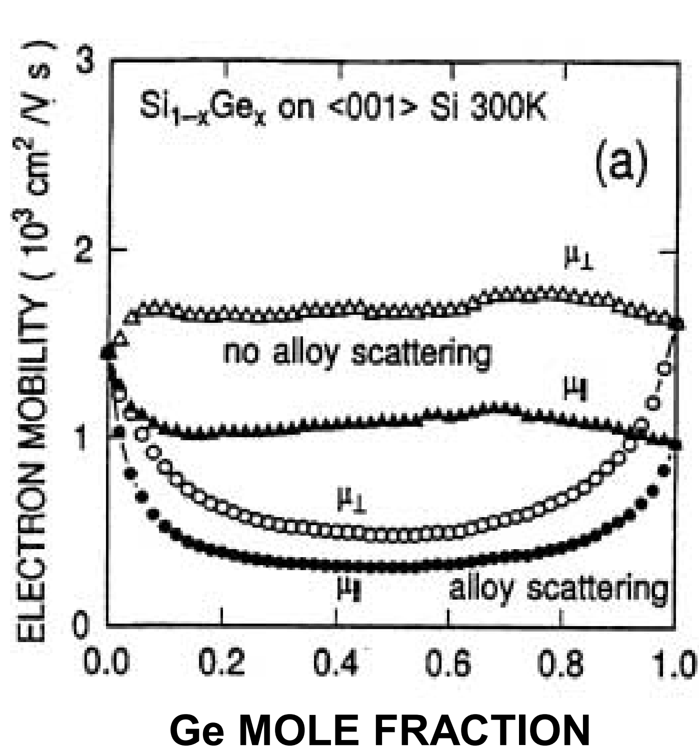
Si-based Strained Materials



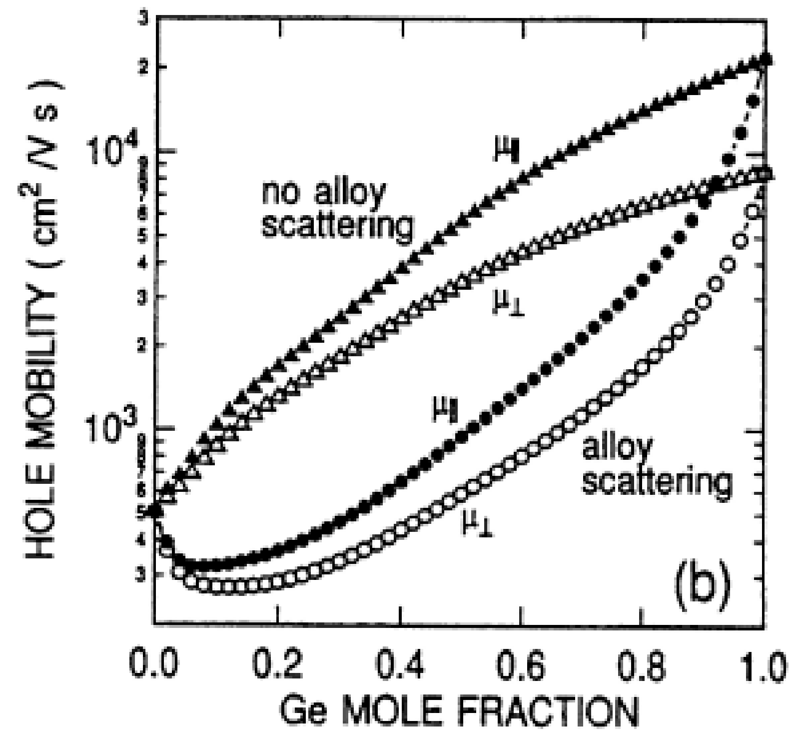
Calculated Electron and Hole Mobility of Strained SiGe

Hole mobility with/without alloy scattering in plane and out-of-plane

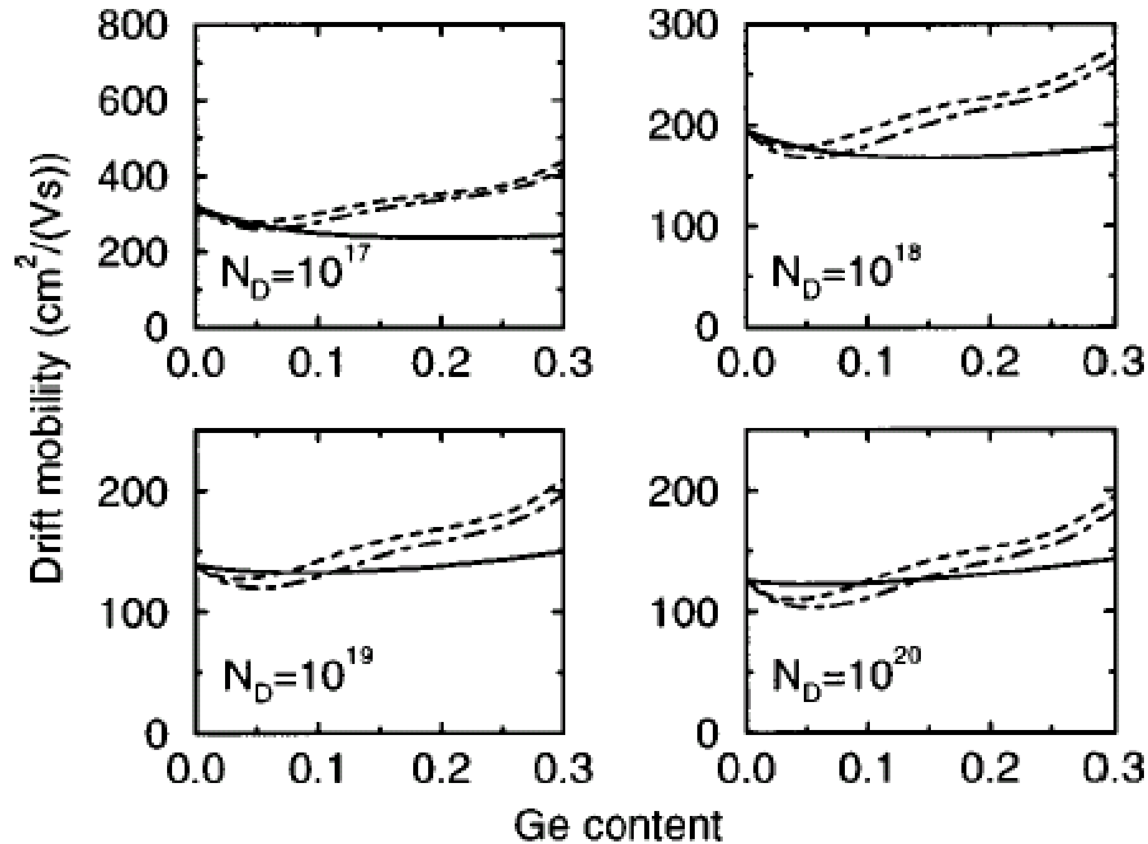
Electron mobility with/without alloy scattering in plane and out-of-plane



Ge MOLE FRACTION



Fischetti and S.E. Laux, J. Appl. Phys. 80 (4), 1996

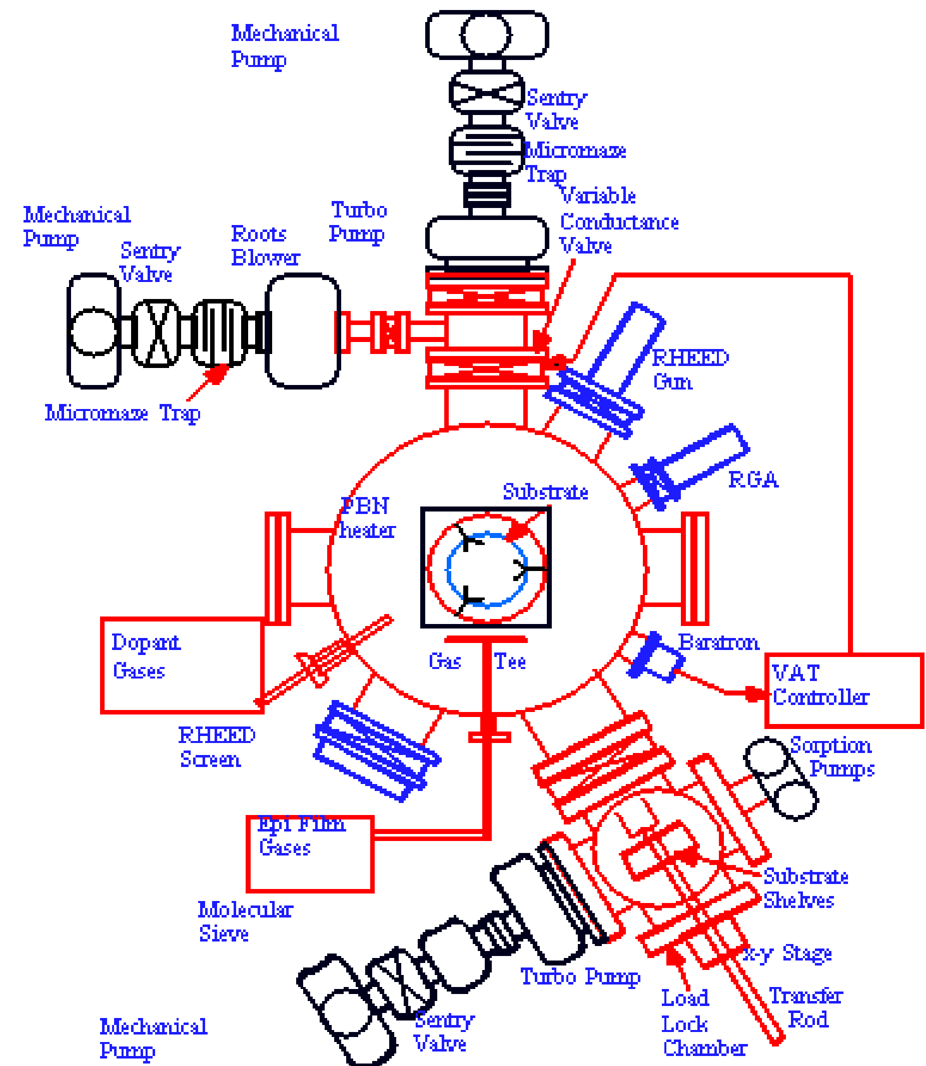


Monte Carlo calculations of minority hole mobilities in $Si_{1-x}Ge_x$ for four doping levels (in cm^{-3}) at 300 K: dot-dashed line is the vertical mobility of strained $Si_{1-x}Ge_x$, solid line is the mobility of unstrained $Si_{1-x}Ge_x$, dashed line is the planar mobility of strained $Si_{1-x}Ge_x$.

FM Bufler, P Graf, B Meinerzhagen, G Fischer, H Kibbel. Hole transport investigation in unstrained and strained SiGe. J. Vac. Sci. Technol. B 16(3), pp. 1667-1669, 1998.

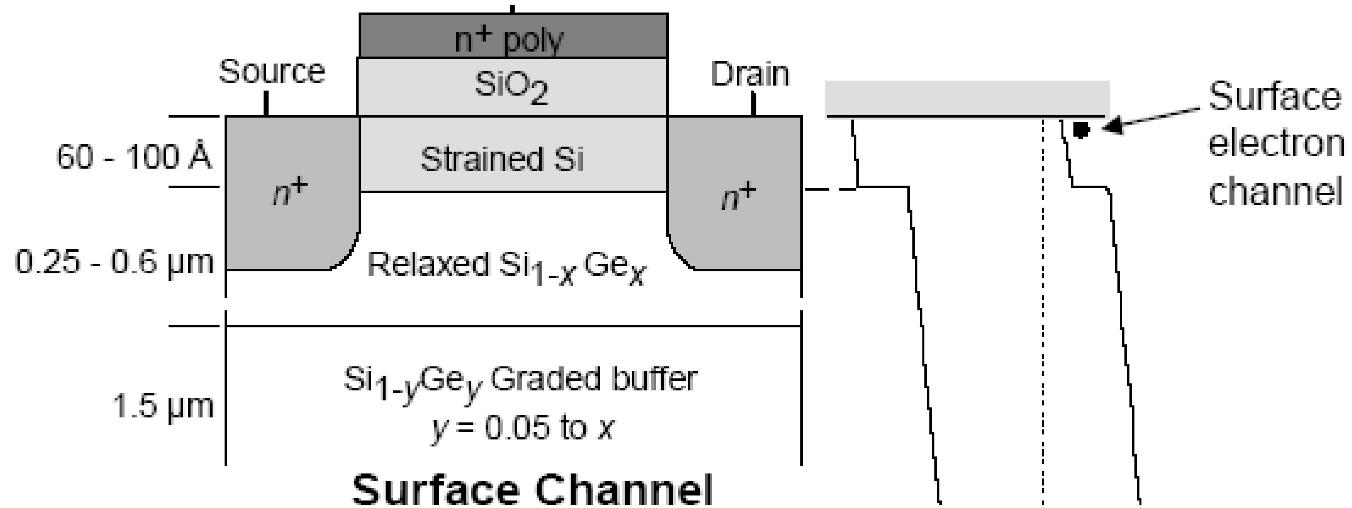
Ultra High Vacuum Chemical Vapor Deposition

- **Base pressure: ~10^{-10} Torr**
- **Cold wall, load locked system**
- **Low deposition pressures**
  - **1 to 10 mTorr**
- **~500° C growth temperature**
  - **Gases**
    - **Si_2H_6, GeH_4, CH_3SiH_3**
    - **B_2H_6, PH_3**



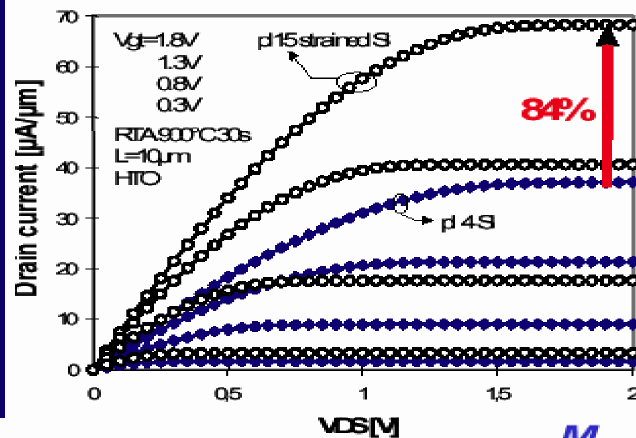
- **Can use hot wall UHVCVD or RTPCVD**

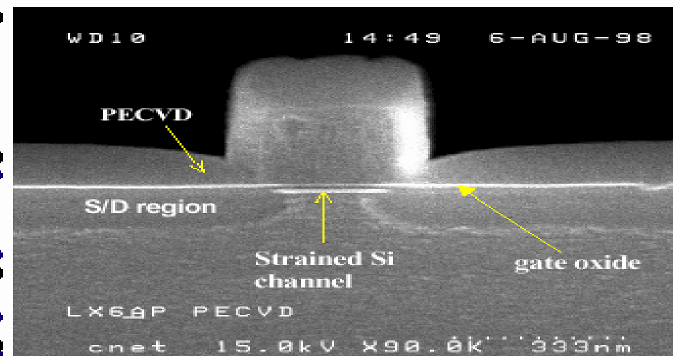
Enhanced-Mobility Strained-Si n-MOSFETs



Welser, et al. IEDM 1992

HIGH MOBILITY DEVICES - STRAINED Si CHANNELS:



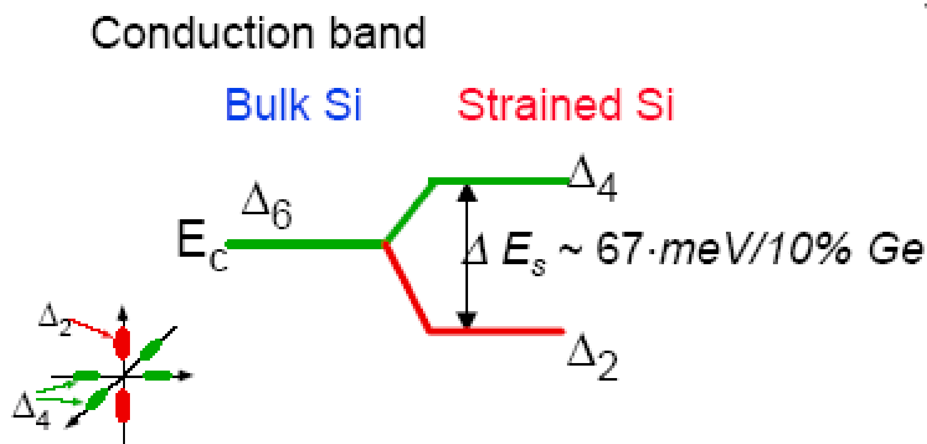


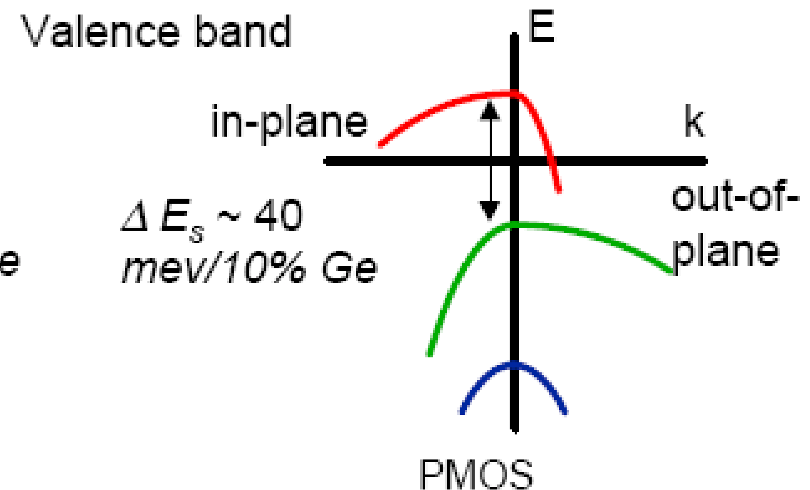
M. Jurczak et al., ESSDERC 1999

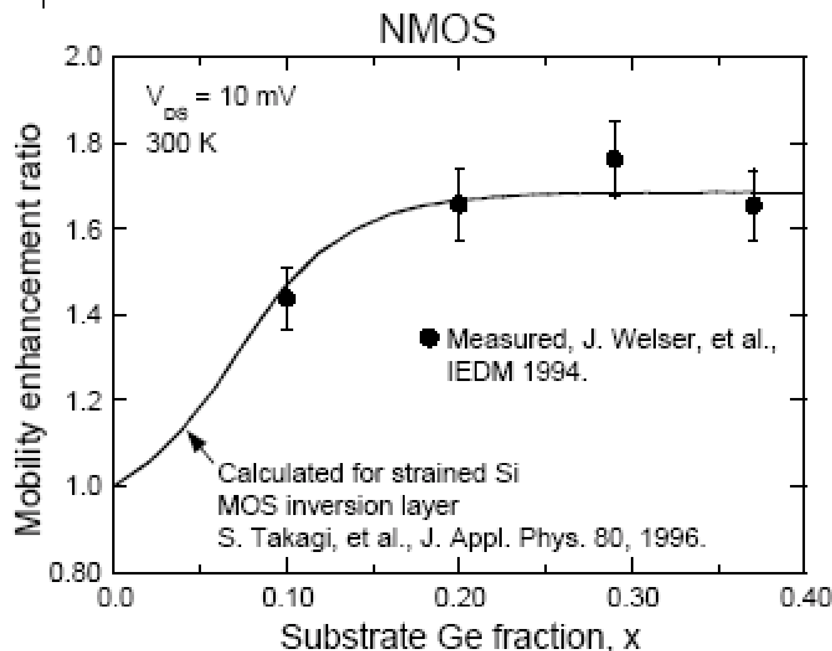
SEMICON Europa 2001 - Slide 26

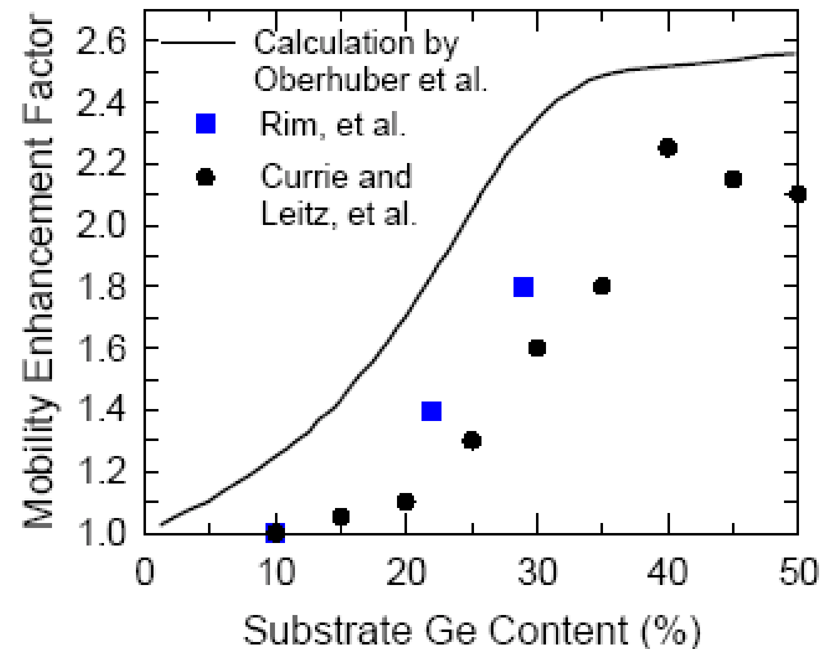
Strained Si-on-SiGe Buffer

Mobility Enhancements in Surface-channel Strained-Si MOSFETs

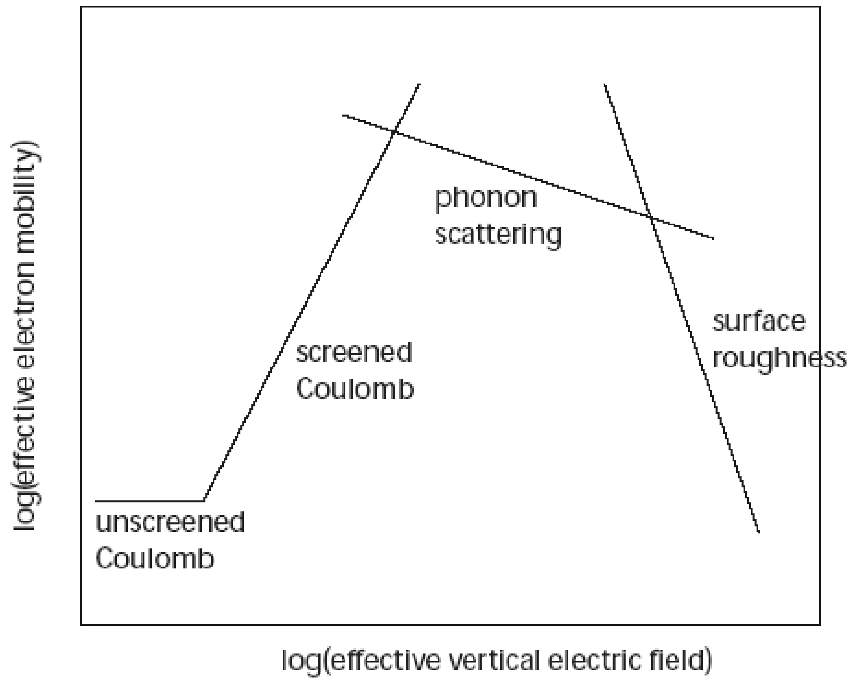








Inversion Layer Mobility



$$E_{eff} = \frac{\frac{1}{2}Q_i + Q_b}{\varepsilon_s}$$

Strained Si mobility enhancement may be due to reduced surface roughness, rather than bandstructure (Fischetti)

Matthiessen's rule:

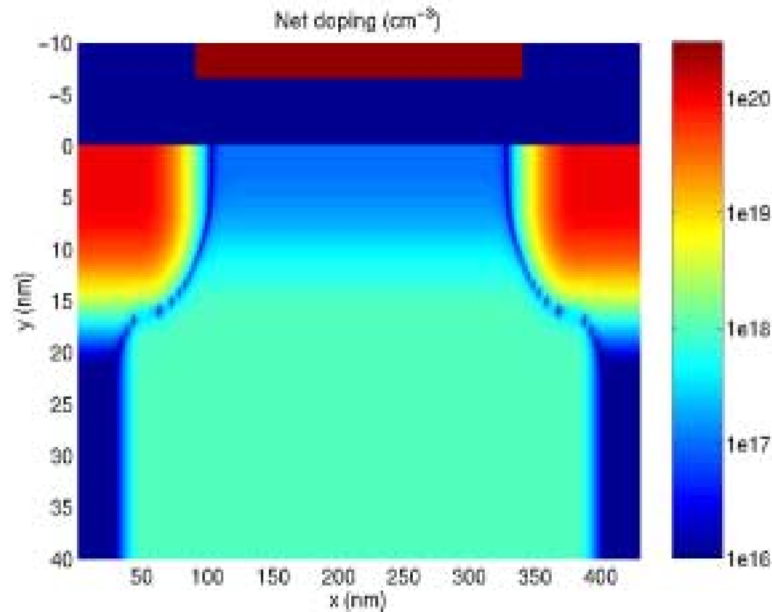
$$\frac{1}{\mu} = \frac{1}{\mu_{Coulomb}} + \underbrace{\frac{1}{\mu_{phonon}} + \frac{1}{\mu_{surface-roughness}}}_{\frac{1}{\mu_{universal}}}$$

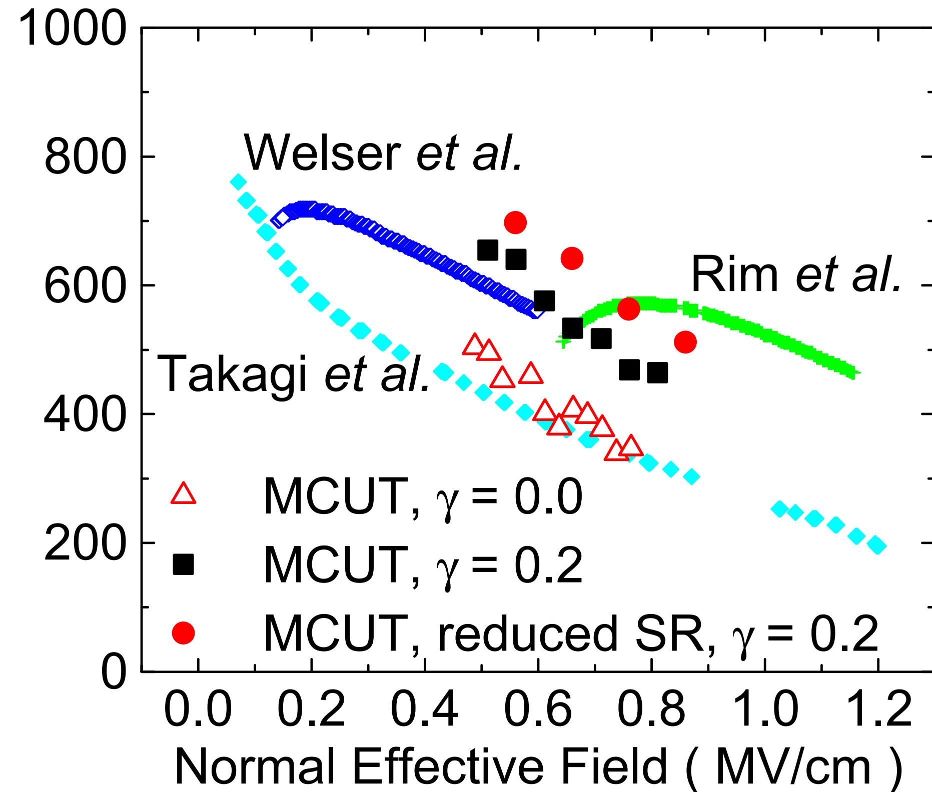
- Doping dependent mobility model incorporated into existing mobility model in MEDICI device simulator.

(Lombardi, et al.)

$$\mu_{coulomb} = An^{\alpha}N_a^{-\beta} \quad \mu_{sr} = \frac{\delta}{E_{\perp}^2} \quad \mu_{phonon} = \frac{\alpha}{E_{\perp}} + \frac{\beta N_a^{0.0284}}{T(E_{\perp})^{1/3}}$$

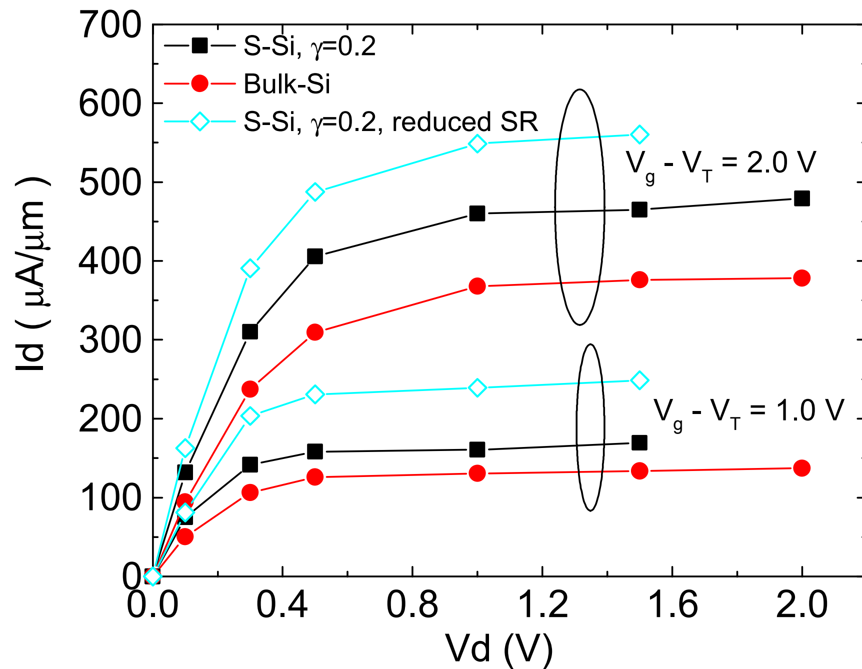
Strained Si NMOSFET Monte Carlo Simulations

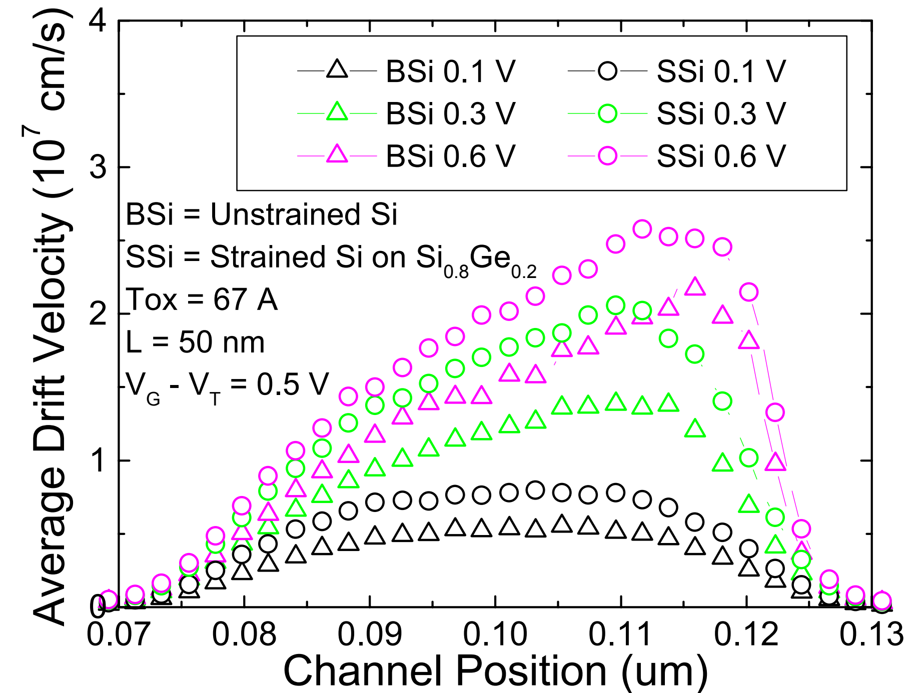




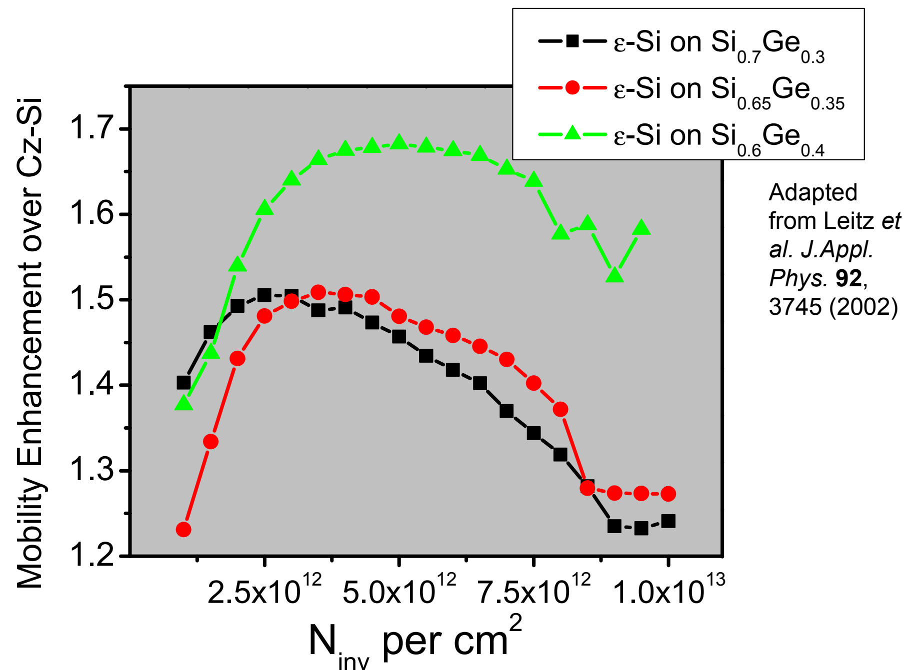
- ➢MOSFET (Tox= 2 nm) K. K. Rim *et. al.*, IEEE Trans. on Elec. Dev., 47 (7), pp. 1406, 2000
- ➢ MIT well-tempered device structure:http://www-mtl.mit.edu/Well/device50/topology50.html
- ➢1-D Schrödinger equation for quantum correction
- ➢As suggested by Fischetti et. al., J. Appl. Phys., 92 (12), 2002), surface roughness reduction may play a role in mobility increase in strained-Si devices.

Current enhancement in Strained Si NMOSFET





Strained Si p-MOSFETs



Adapted from Leitz *et al. J.Appl. Phys.* **92**, 3745 (2002)

*Lee and Fitzgerald, MARCO, 2004

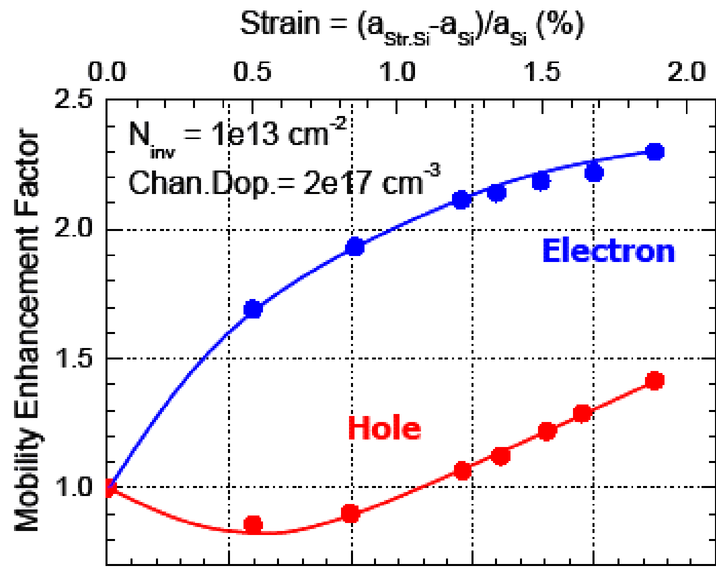
*Rim et al. *IEDM* (1995).
Nayak et al. *IEEE Trans. on Elec. Dev*. **43**, 1709 (1996)

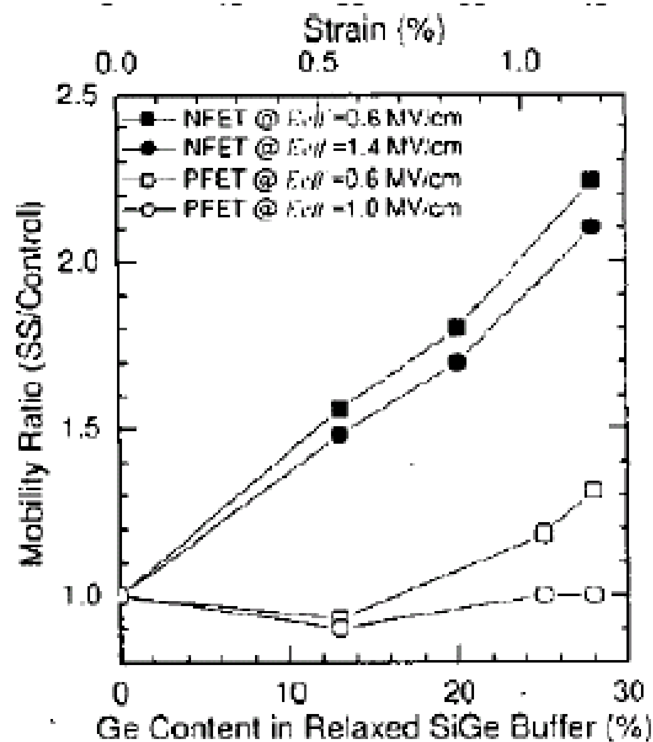
**Rim *et al. Symposium on VLSI Technology* (2002)

- μ_{eff} enhancement *decreases* with gate overdrive* for holes
  - No *p*-channel enhancement at E_{eff} = 1 MV/cm** for x = 0.28
  - Physical mechanism poorly understood

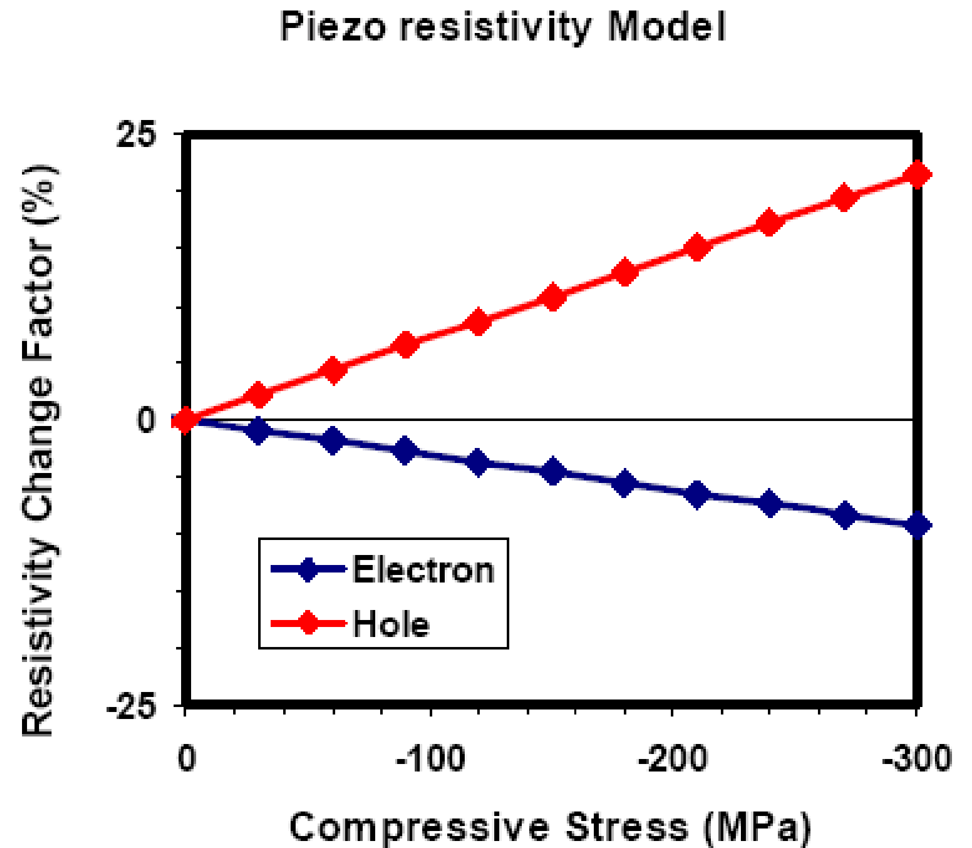
Performance benefits of ε-Si primarily from *n*-MOSFET

Mobility enhancement in tensile and compressively strained Si





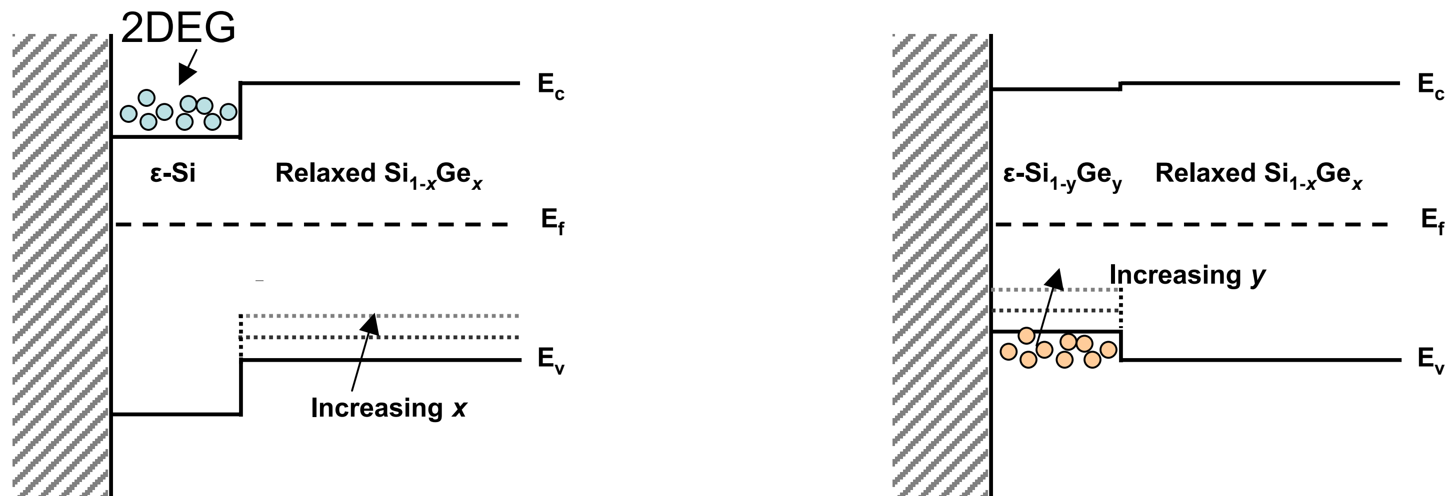
Rim /IBM



Mobility with Strain *(Courtesy: Yu)*

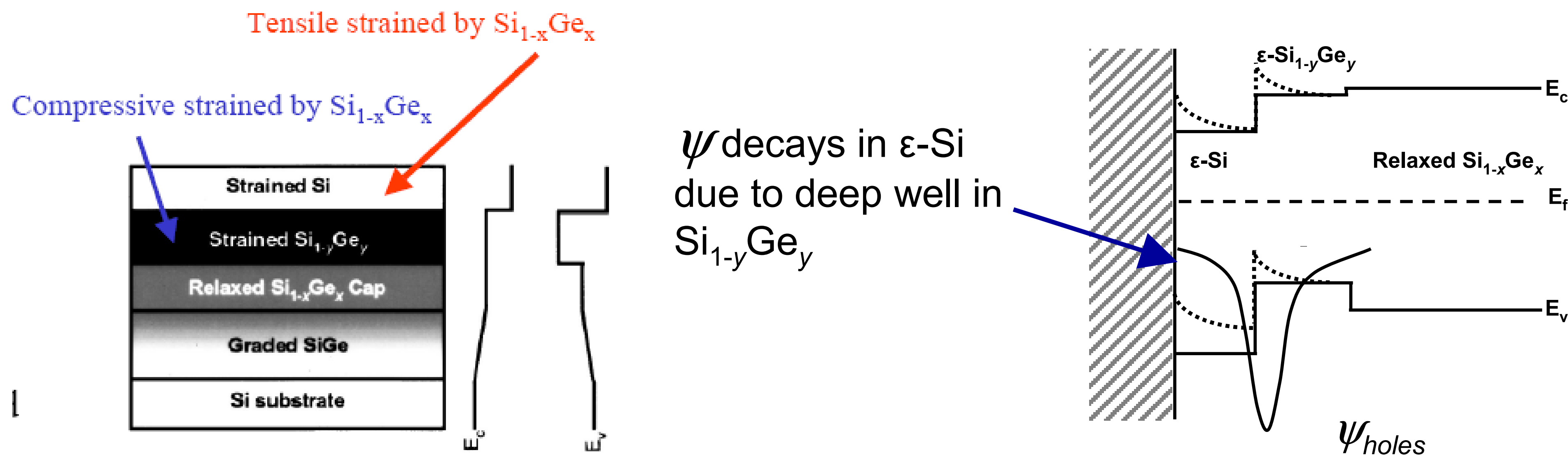
	Compressive	Un-strained	Tensile
Si	e: degraded p: enhanced	-	e: enhanced p: degraded (stress<1MPa) p: enhanced (stress>1MPa)
SiGe	e: degraded p: enhanced	e: degraded (Ge<0.8) e: enhanced (Ge>0.8) p: degraded (Ge<0.7) p: enhanced (Ge>0.7)	e: enhanced (Ge<0.2) e: degraded (Ge>0.2) p: enhanced (Ge<0.3) p: degraded (Ge>0.3)

SiGe strain- and band-engineered heterostructures



- Relaxed $Si_{1-x}Ge_x$ virtual substrates allow
  - Si-rich alloys in biaxial tension ($a_{\parallel}/a_o > 1$)
    - Type-II band offset → Two-dimensional electron gas
    - Barrier for holes
  - Ge-rich alloys in biaxial compression ($a_{\parallel}/a_o < 1$)
    - Type-I band offset → Two-dimensional hole gas
    - Cannot confine electrons

Dual-channel heterostructures



x = 0.2, y = 0.5 or x = 0.3, y = 0.6

- Cannot confine ψ in one channel or another
  - Different from traditional buried-channel device
- ε-$Si_{1-y}Ge_y$ layer beneath ε-Si boosts μ_{eff} even at large N_{inv}, high E_{eff}
- ε-Si is more than just a “cap”
  - Enhanced hole mobility*, different from pseudomorphic SiGe devices

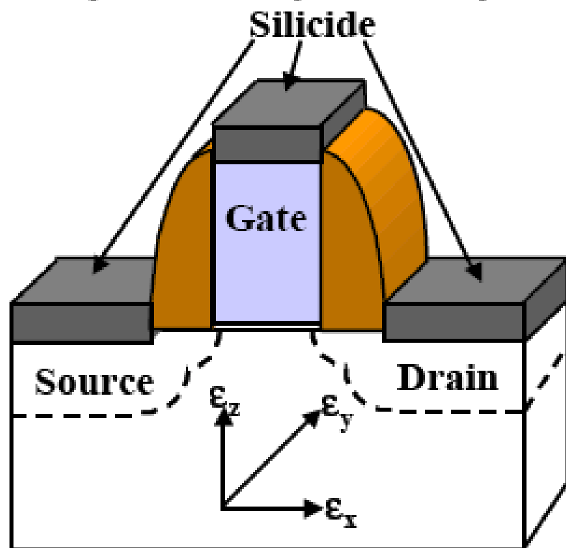


Figure 1 Schematic view of 3D process-induced strain components.

TABLE I Impact of 3D Strain Effects on CMOS Performance.
*Strain change = Increased tensile or decreased compressive strain

Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

3D Strain Sensitivity of CMOS Current Drive

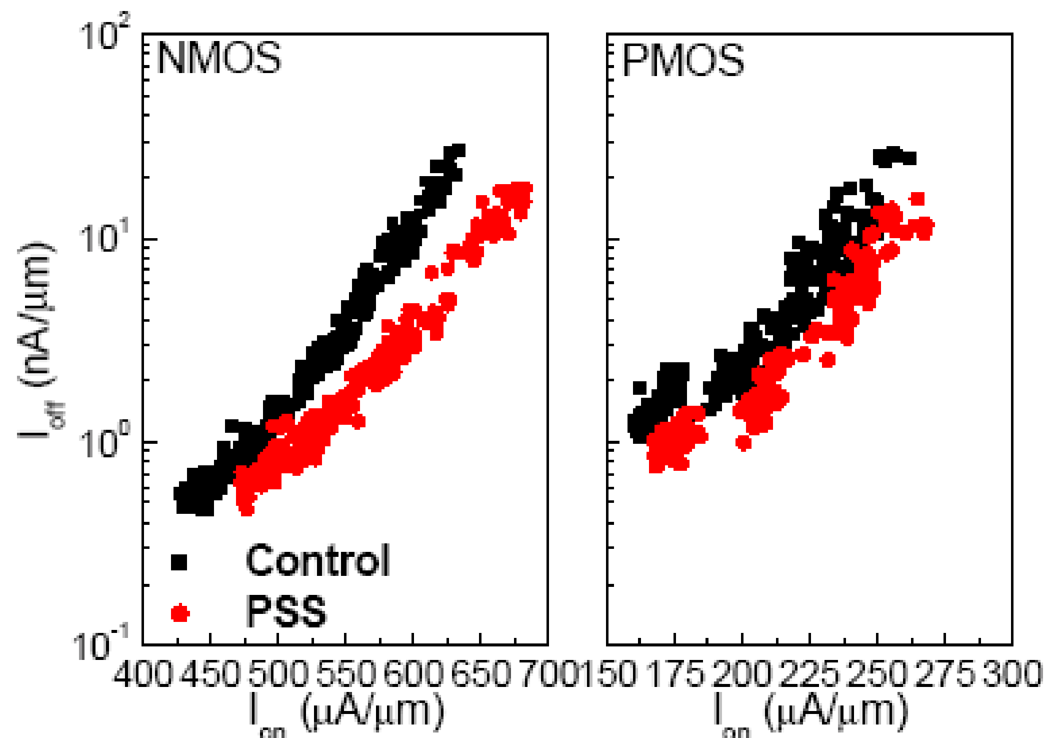
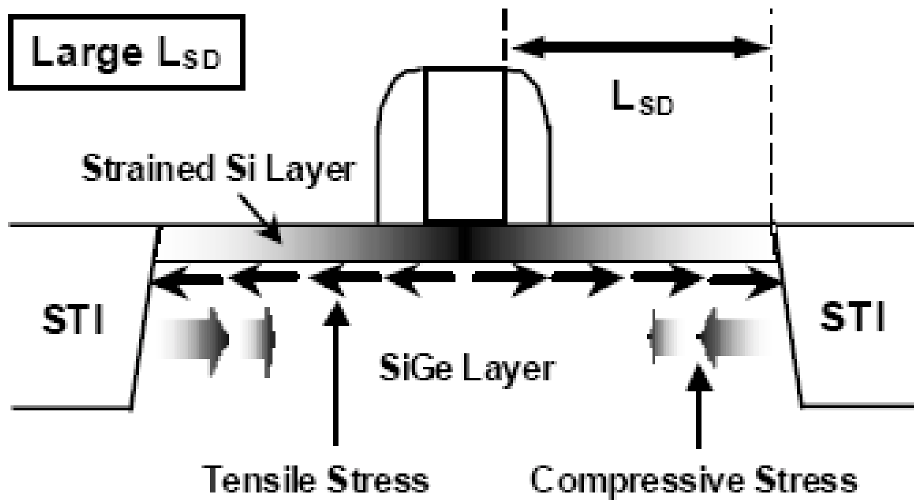
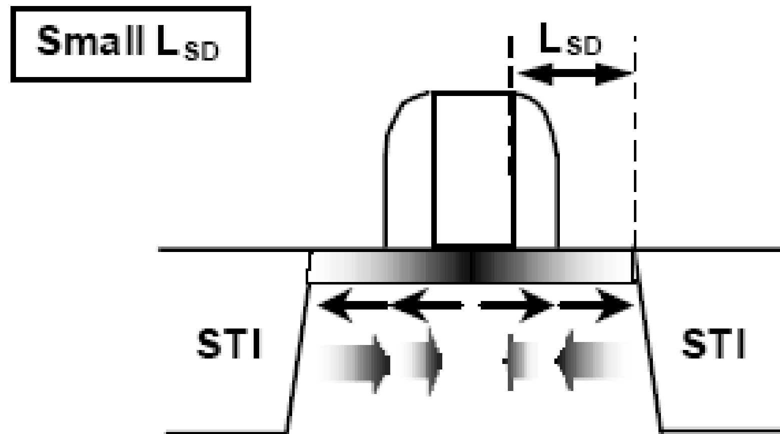
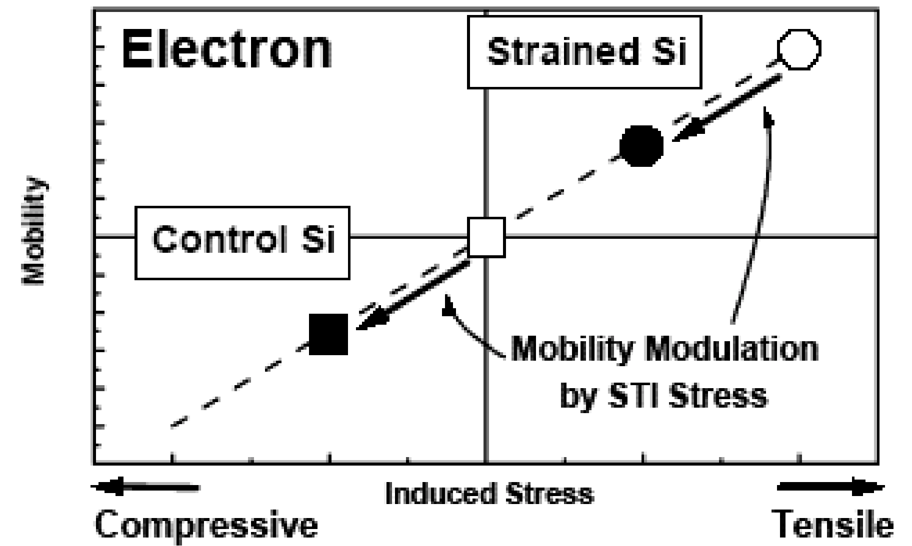


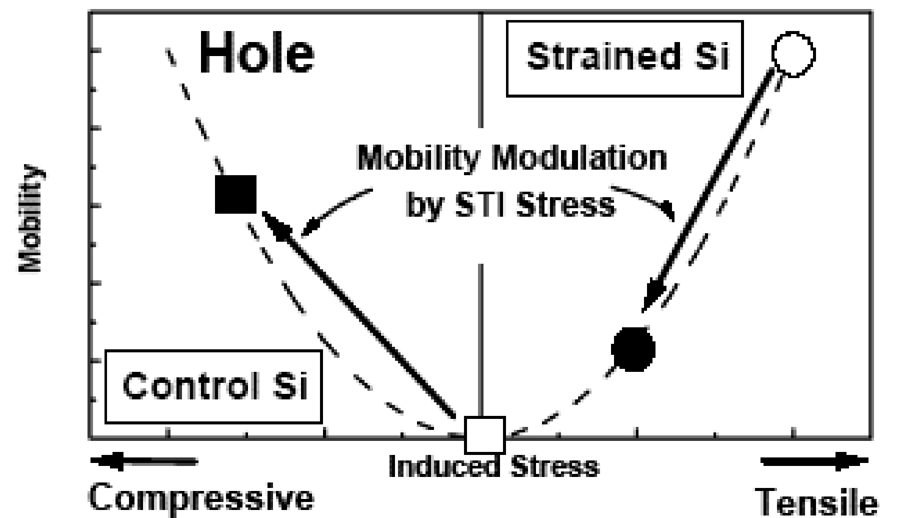
Figure 3 I_{on} vs. I_{off} characteristics at 1V operating voltage. Up to 15% improvement is achieved in NMOS and PMOS with cap-layer-, STI- and silicide-strained Si.

Ge, et. al, IEDM 2003



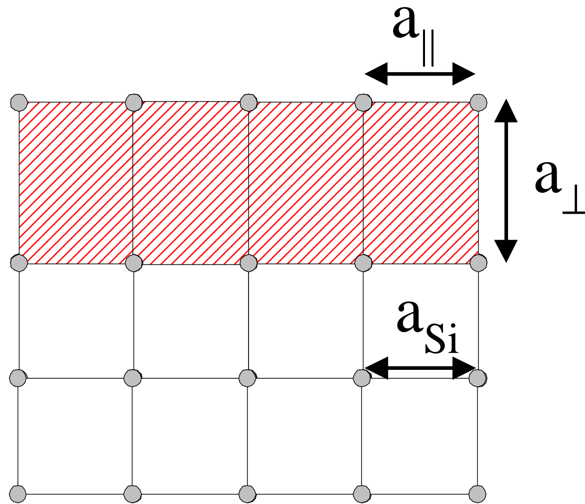


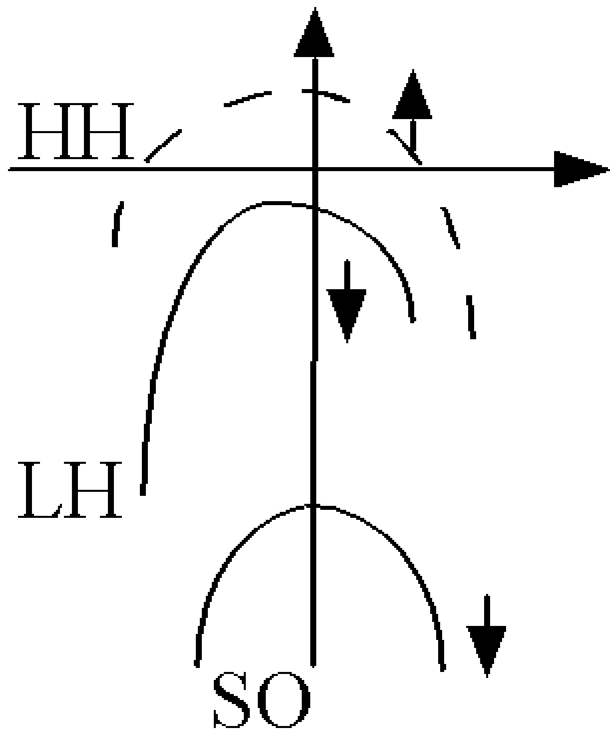


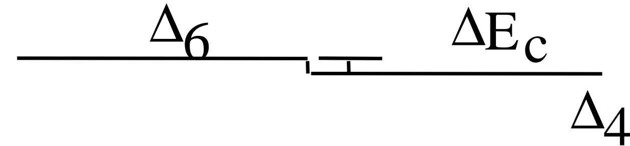


Sanuki, et. al. IEDM 2003

Electronic Properties of Strained $Si_{1-x}Ge_x$

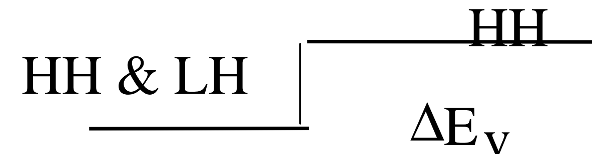






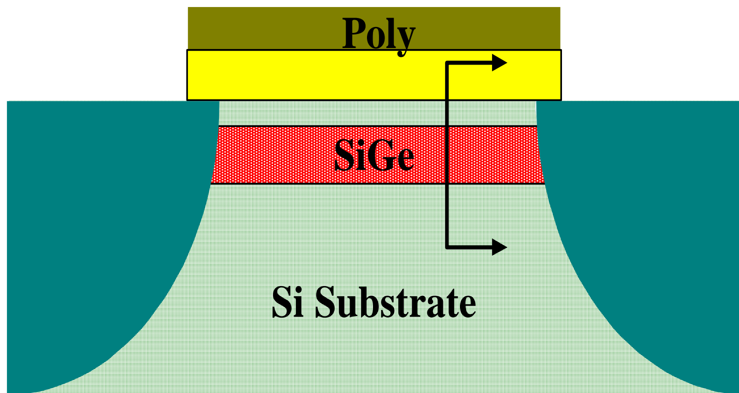
Relaxed Si

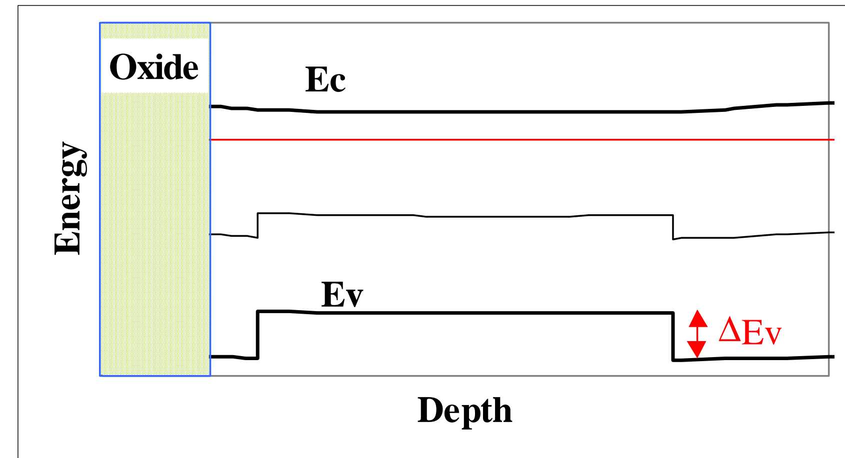
Strained $Si_{1-x}Ge_x$



Type-I (Compressive)

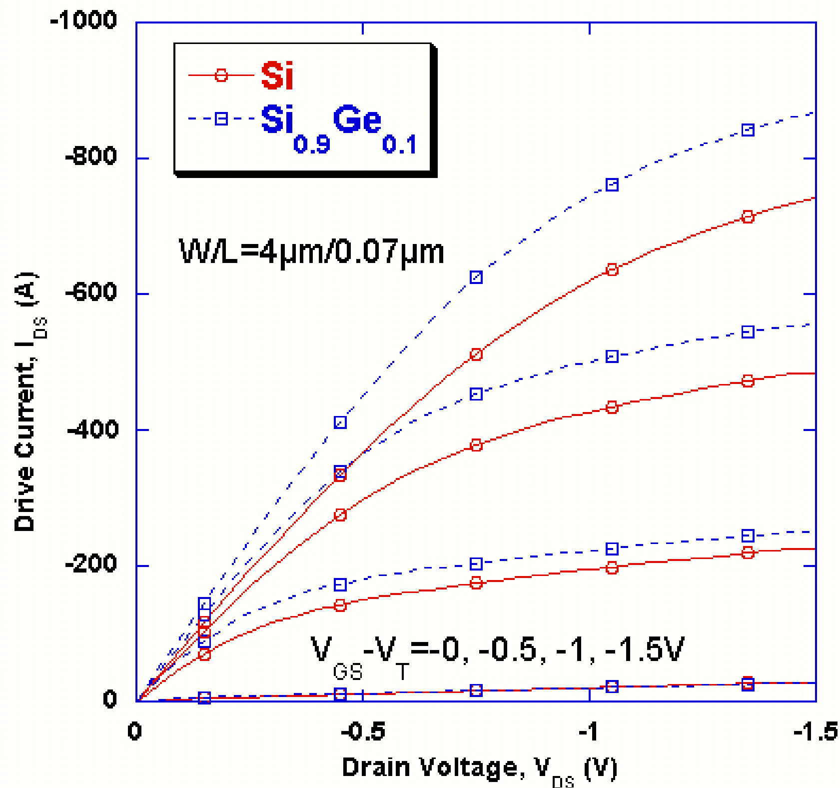
SiGe MOSFET Structure

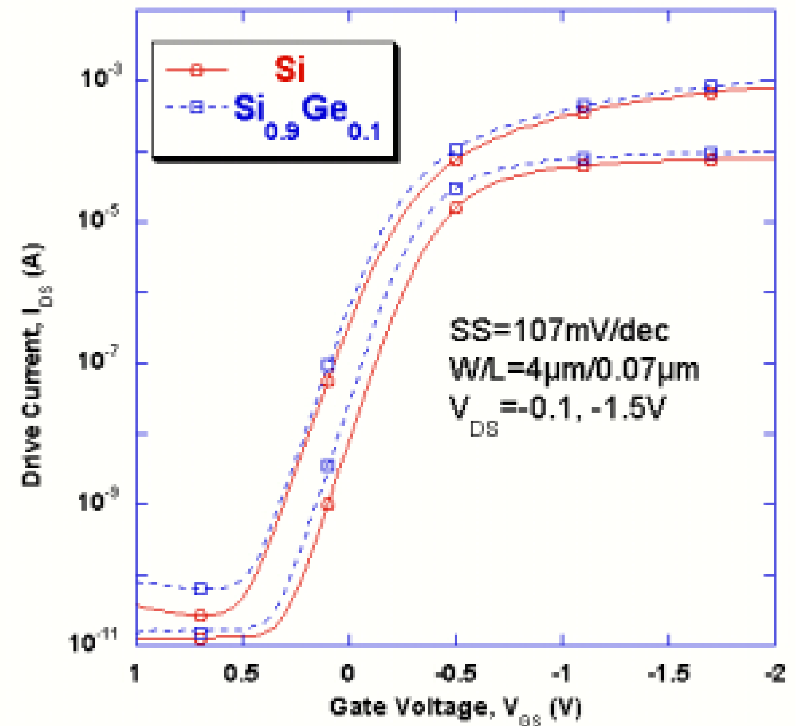




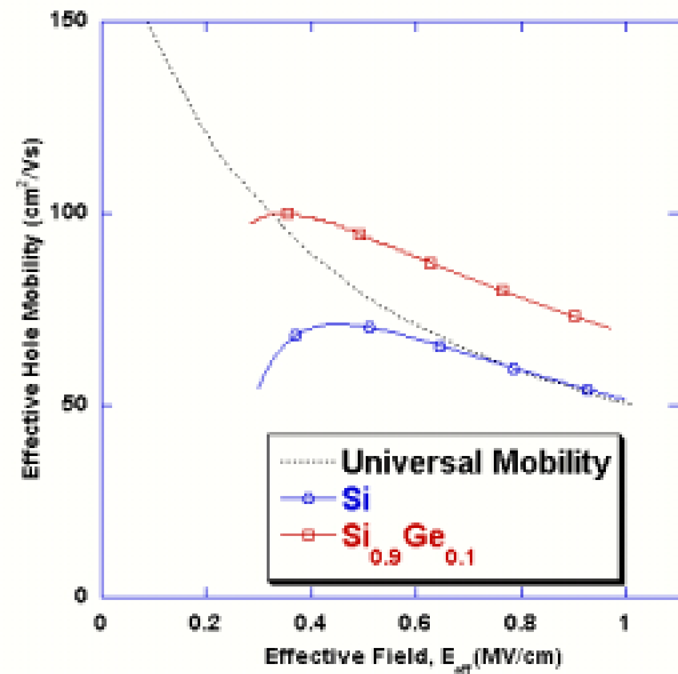
- Typical MOS structure
  - $Si_{1-x}Ge_x$ channel with Si cap leads to buried channel, and lower gate capacitance
- Si cap
  - Used for oxidation
  - Also acts as a parasitic channel, leading to gate operating "window"

Z.Shi, ..S. Banerjee "Simulation and optimization of strained Si1-xGex buried channel p-MOSFETs," Solid State Electronics, 44 (7): 1223, 2000.

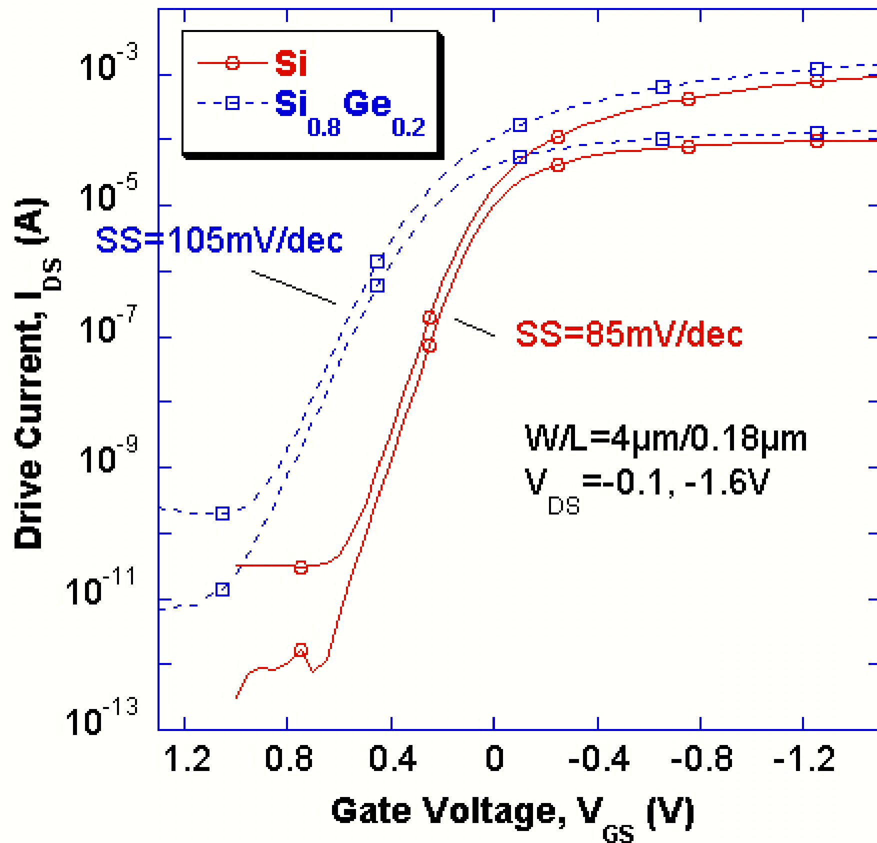


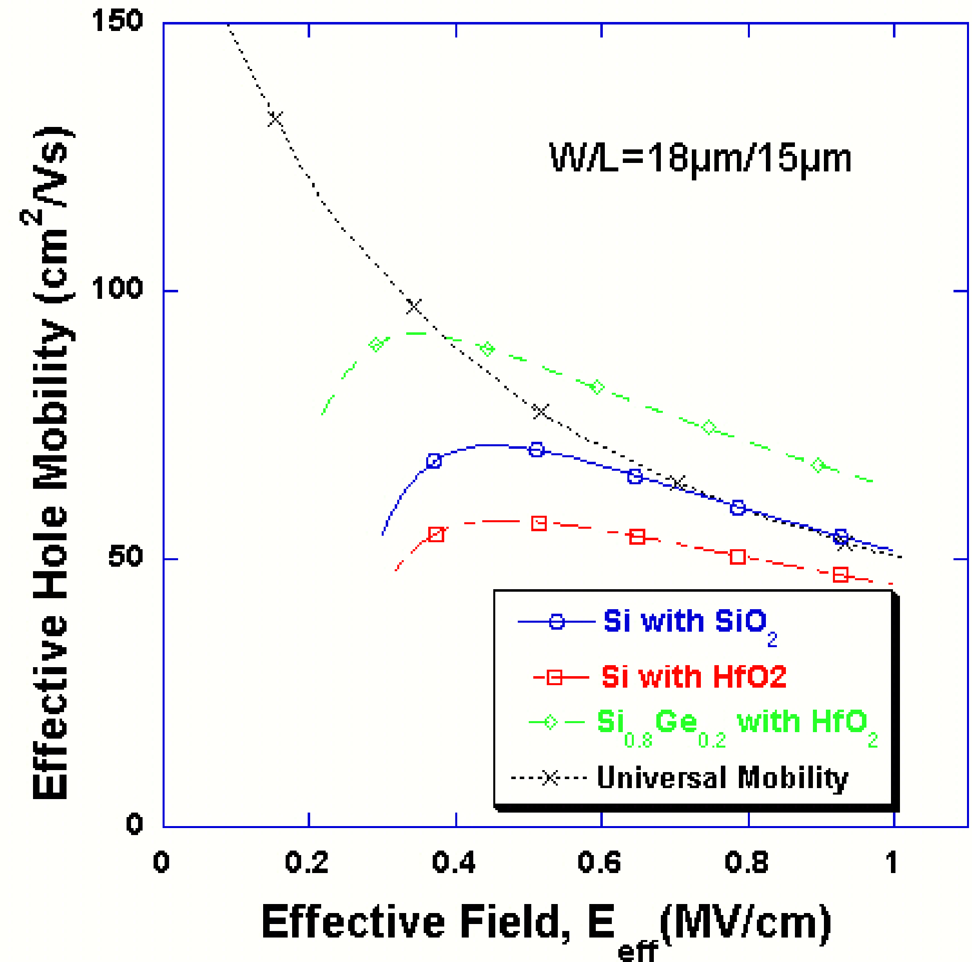


Output, sub-threshold, and mobility-field characteristics of 70nm $Si_{0.9}Ge_{0.1}$-SiO_2 buried channel PHFET.



E. Quinones,..S.Banerjee "Design, Fabrication, and Analysis of SiGeC Heterojunction PMOSFETs," IEEETrans.Elec.Dev., Sept. 2000.





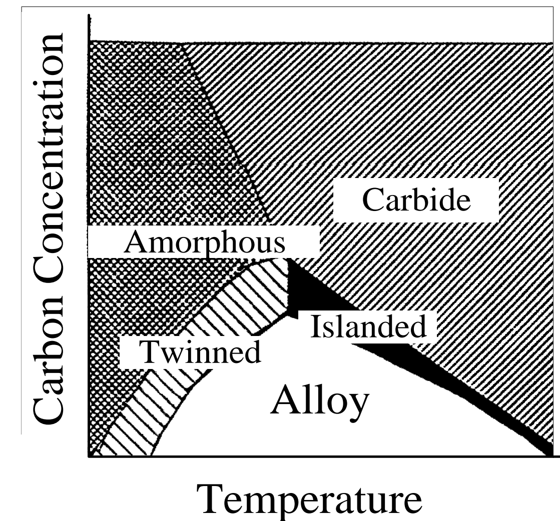
Subthreshold and mobility-field characteristics for 180nm $Si_{0.8}Ge_{0.2}$-HfO_2 PHFETs and control Si PMOSFET.

Recovery of mobility degradation for high-k gate dielectrics with enhanced-mobility channels: *(Onsongo,.., Banerjee)*

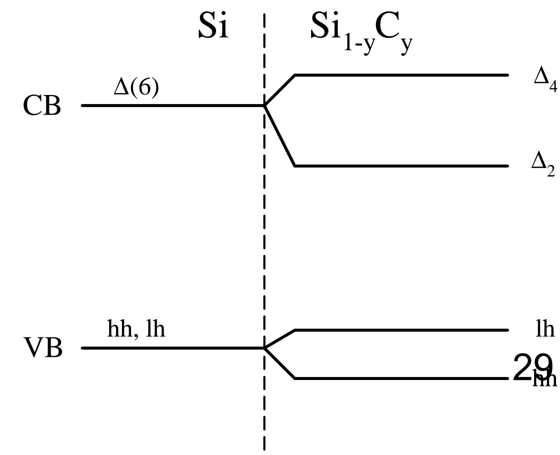
T.Ngai, J.Lee, S.Banerjee, "Electrical Properties of ZrO2 Gate Dielectric on SiGe," Appl. Phys. Lett., 76(4), p. 502, Jan. 2000.

Addition of C to Si and $Si_{1x}Ge_x$

- Carbon has a smaller lattice constant
  - Strain compensation of SiGe (~8:1)
  - Tensile strained Si-C on Si
- Low solubility in Si
  - Need low temperature growth to incorporate C due to low solubility ($5x10^{17}$ cm^{-3})
  - Growth window for alloy growth
- Carbon ΔE_v=21-26meV/%C in SiGeC (Lanzerotti, EDL,1996)
  - Ge ΔE_v=25 meV/3% Ge
- Carbon ΔE_c=75-90 meV/%C for SiC
  - (Faschinger, APL, 1995)

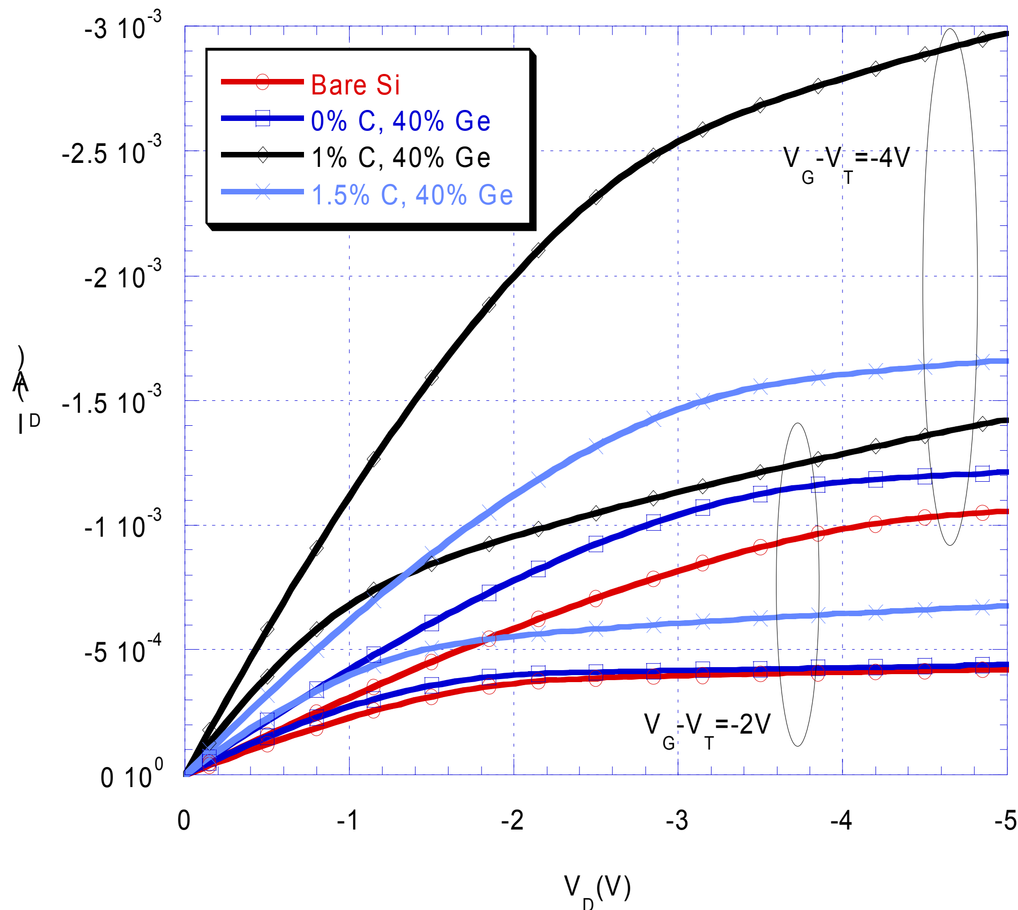


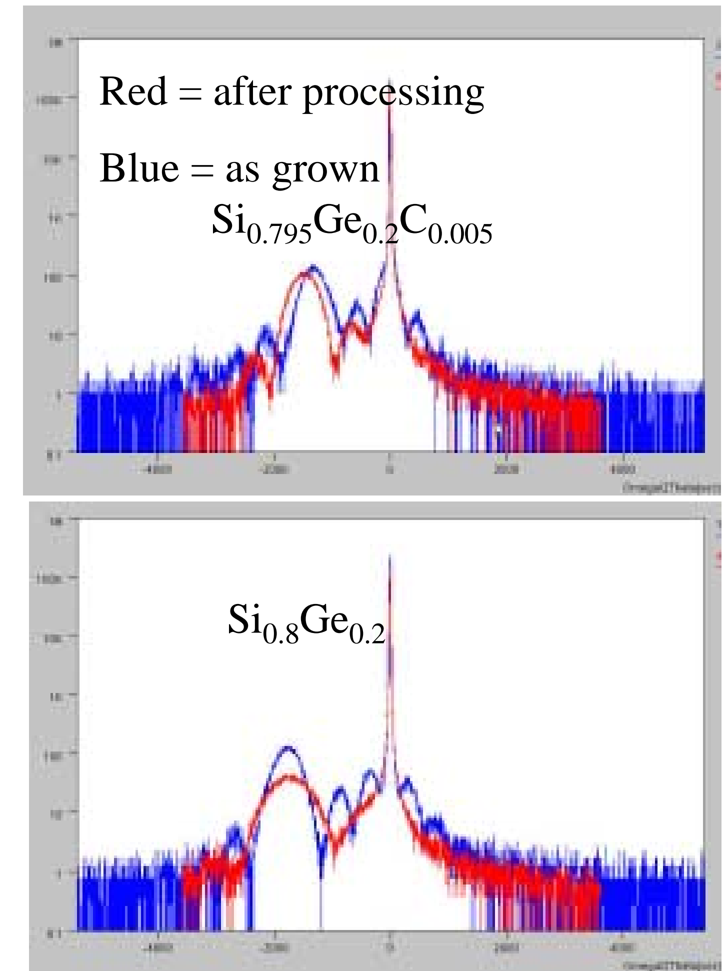
A. R. Powell, K. Eberl, B. A. Ek, and S. S. Iyer, "$Si_{1-x-y}Ge_xC_y$ growth and properties of the ternary system," Journal of Crystal Growth Vol. 127, pp. 425, 1993.



K. Eberl, K. Brunner, W. Winter, "Pseudomorphic $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ alloy layers on Si," Thin Solid Films, Vol. 294, pp. 98, 1997.

Carbon Strain Compensation





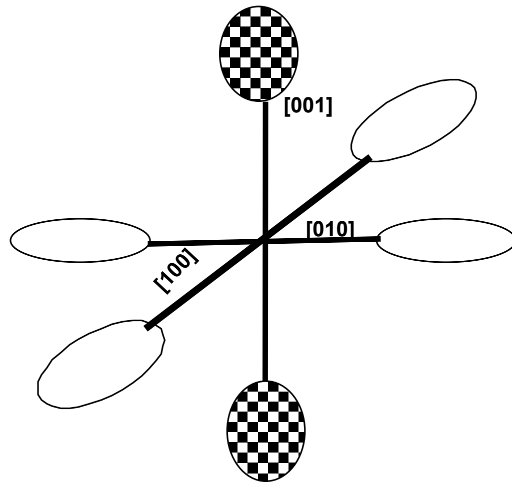
$Si_{0.585}Ge_{0.4}C_{0.015}$ shows 55% drive current enhancement over bulk Si and 42% enhancement over $Si_{0.6}Ge_{0.4}$

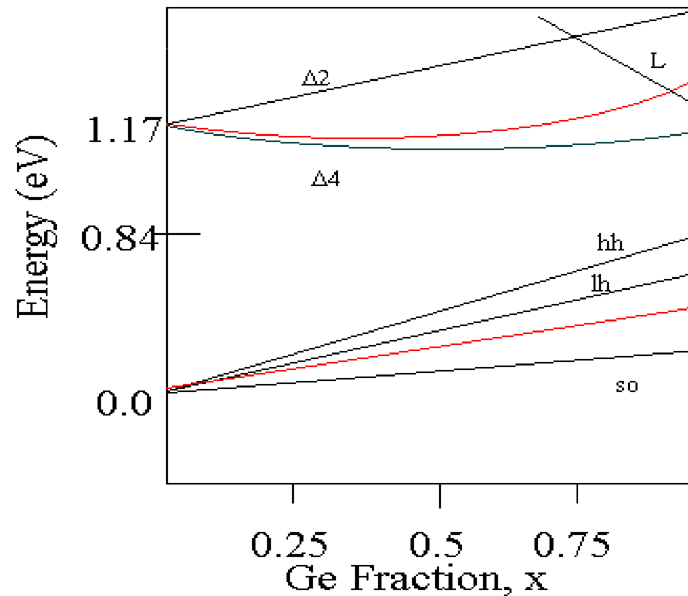
W/L= 10/0.5 um; tox= 6 nm

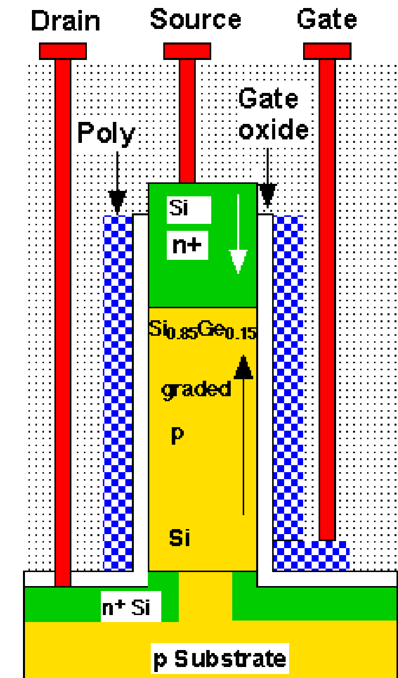
XRD Rocking Curves

S.Ray, .. S.Banerjee, “Novel SiGeC Channel Heterojunction PMOSFET,” *Proc. of Int. Elec. Dev.Meet., 1996.*

Electronic Properties of Strained $Si_{1-x}Ge_x$





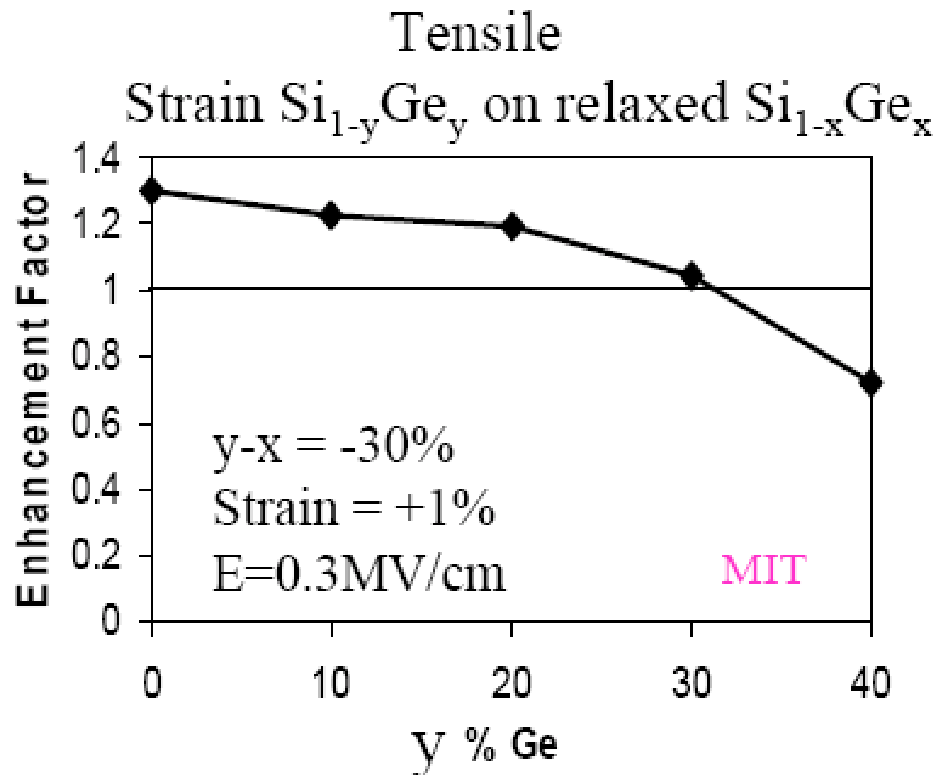


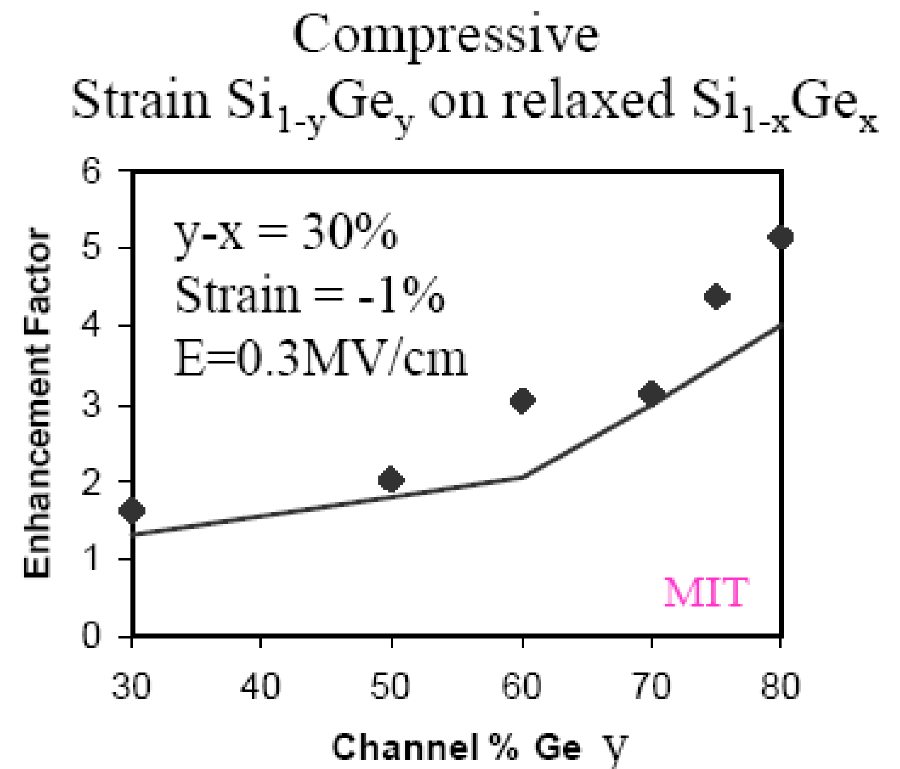
- Strain splits the six fold degeneracy of conduction band valleys.
- The four-fold in-plane valleys are lowered, leading to less f-type scattering.
- Carriers have a lower out-of-plane and higher in-plane mass.
- Electron mobility dependent on directions: increase in ⊥, decrease in ||
- To enhance electron mobility for the planar NMOSFETs, tensile strained Si has to be used.

- Hole mobility increases with Ge fraction.
  - Valence band splitting with strain results in reduced scattering.
  - Reduction of effective hole mass with strain due to VB warpage
  - Increase in both ⊥ and || mobilities

Chen XD,.. Banerjee SK, Hole and electron mobility enhancement in strained SiGe vertical MOSFETs, IEEE T ELECTRON DEV 48 (9): 1975-1980 SEP 2001

Hole mobility in Strained SiGe



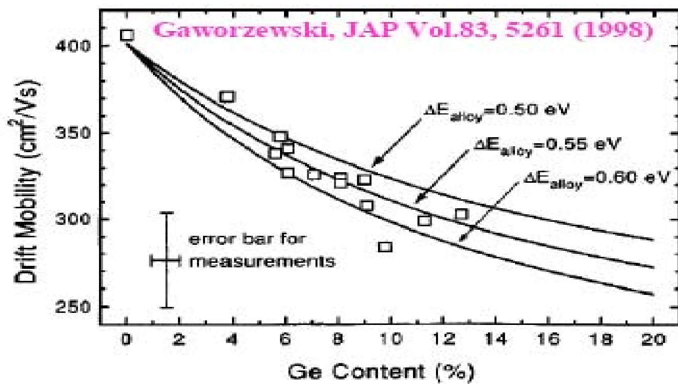


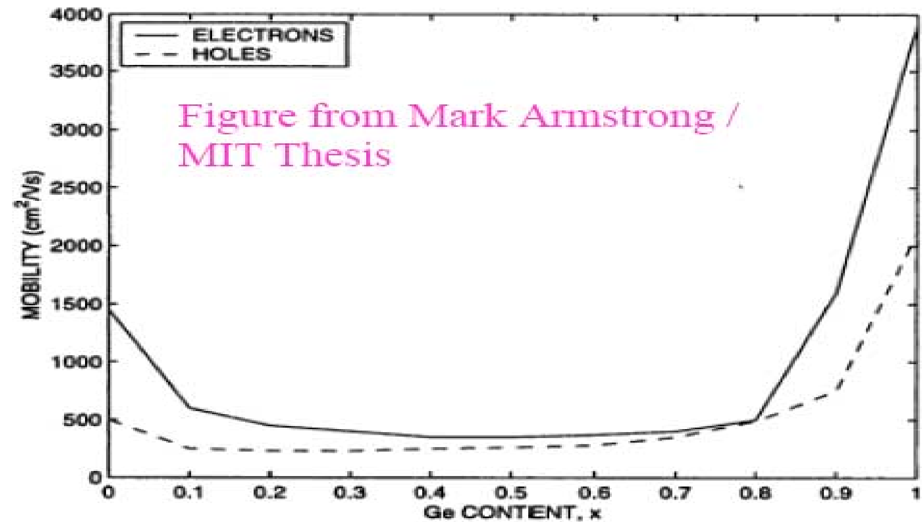
- In tensile SiGe, hole mobility decreases as Ge% increase
- Enhanced below 30% Ge

In compressive SiGe, hole mobility increases as Ge% increase

Mobility in Relaxed SiGe

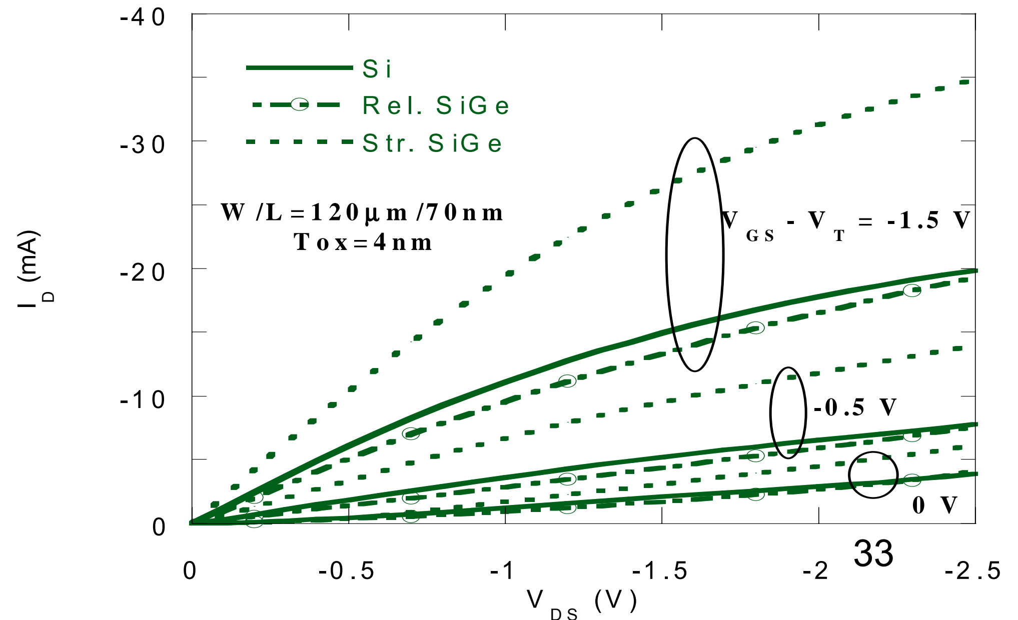
- Mobility degraded for most of Ge%
- Only become higher at >80% Ge
- Alloy scattering is blamed for degradation





Vertical Si, relaxed and strained $Si_{1-x}Ge_X$ PHFETs showing enhancement of drive current over Si MOSFETs only in the presence of strain. *NHFETs also enhanced!*

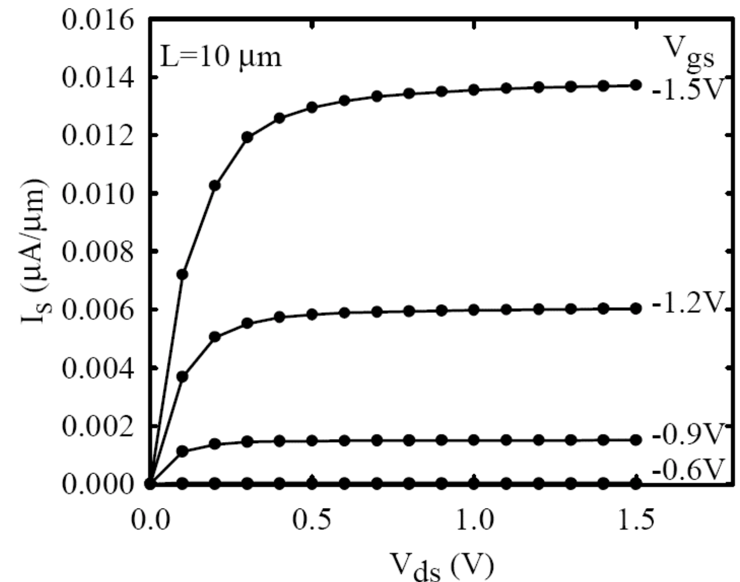
Jayanaran & Banerjee, EMC 2004



Ge MOSFETs

	Ge	Si
μ_n (cm^2/Vs)	3900	1500
μ_p (cm^2/Vs)	1900	450
Eg (eV)	0.66	1.12

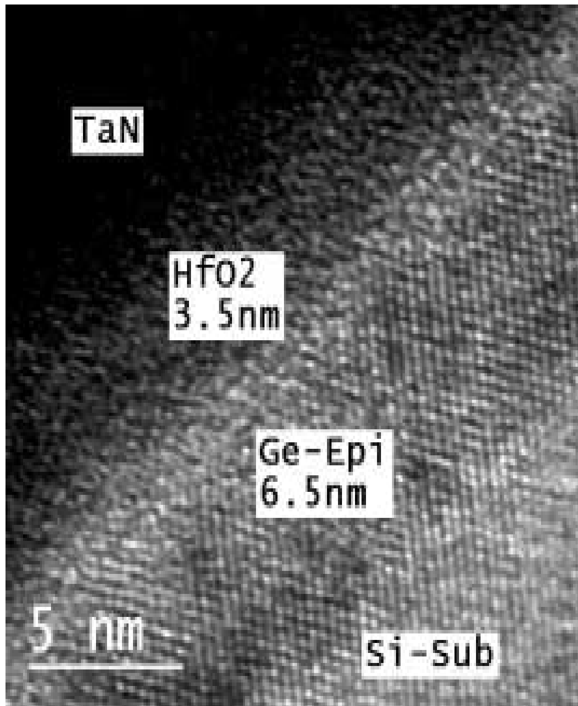
Rosenberg et al. EDL 9, 639 (1988), Shang et al. IEDM(2002), Chui et al. IEDM (2002), Bai et al. VLSI (2003)

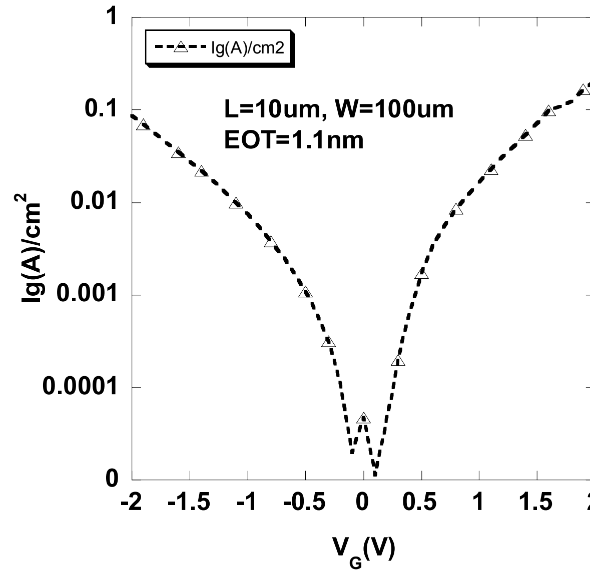


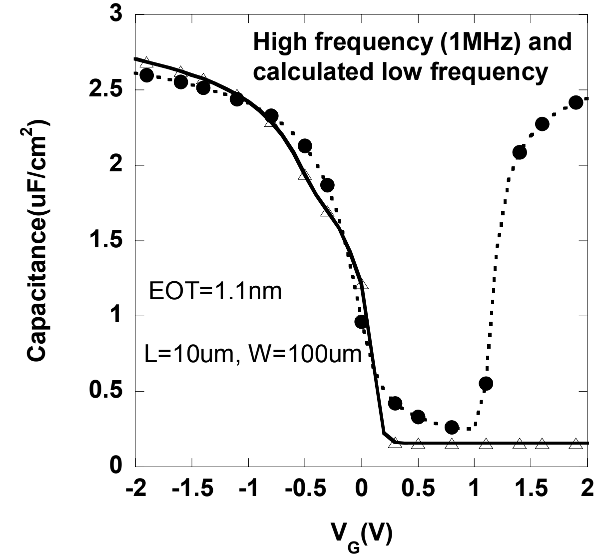
A. Ritenour et al., IEDM, p.433, 2003

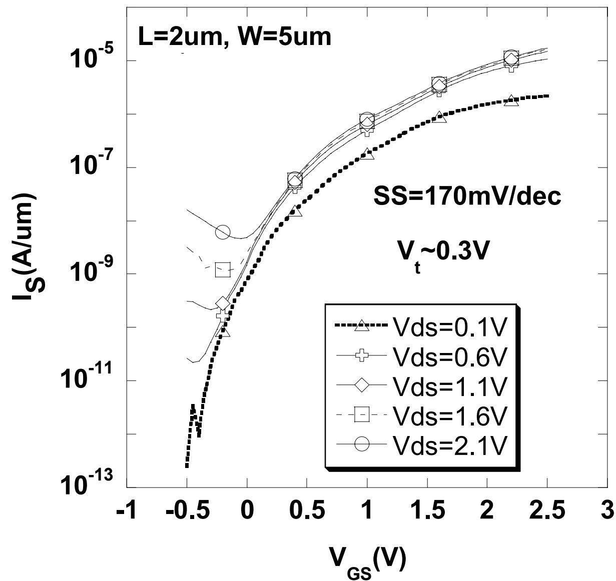
- **Bulk Ge has higher electron (2.5x) and hole (4x) mobility than Si, and can potentially lead to faster MOSFETs and more balanced N vs. PMOSFETs.**
- **Germanium bulk substrates brittle, lower thermal conductivity (0.6W/cm-K vs. 1.5 for Si)**
- **Smaller Ge bandgap than Si broadens absorption spectrum; optoelectronic integration on CMOS?**
- **Native oxide on Ge surface is not stable; GeO_2 water soluble, GeO volatile at low T. Deposited high-k gate dielectrics promising**
- **Performance *much worse than expected*, especially for NMOSFETs, probably because of poor interface between Ge and high-k gate dielectric, as well as poor dopant activation and interface between metal- source/drain**
- **Higher junction leakage in Ge, especially at high T**
- **Higher dielectric constant in Ge leads to worse electrostatics (DIBL, SS)**

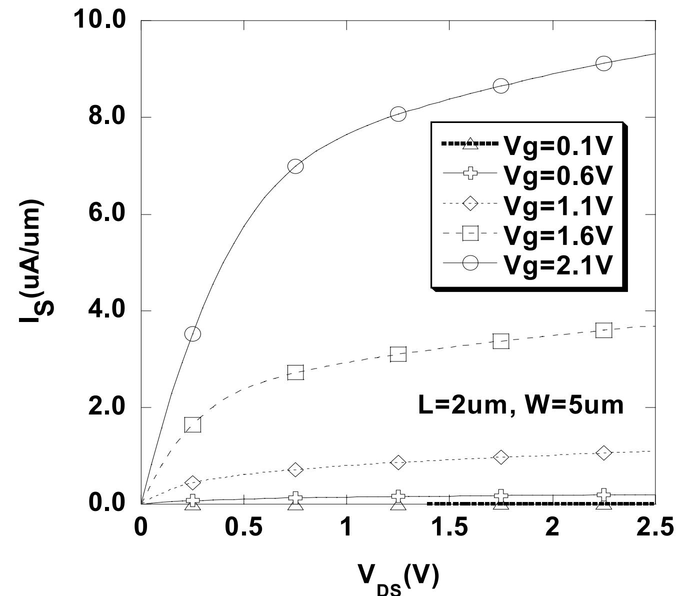
UHVCVD Ge-on-Si NMOS w/o SiGe buffer with PVD HfO2 and TaN gate





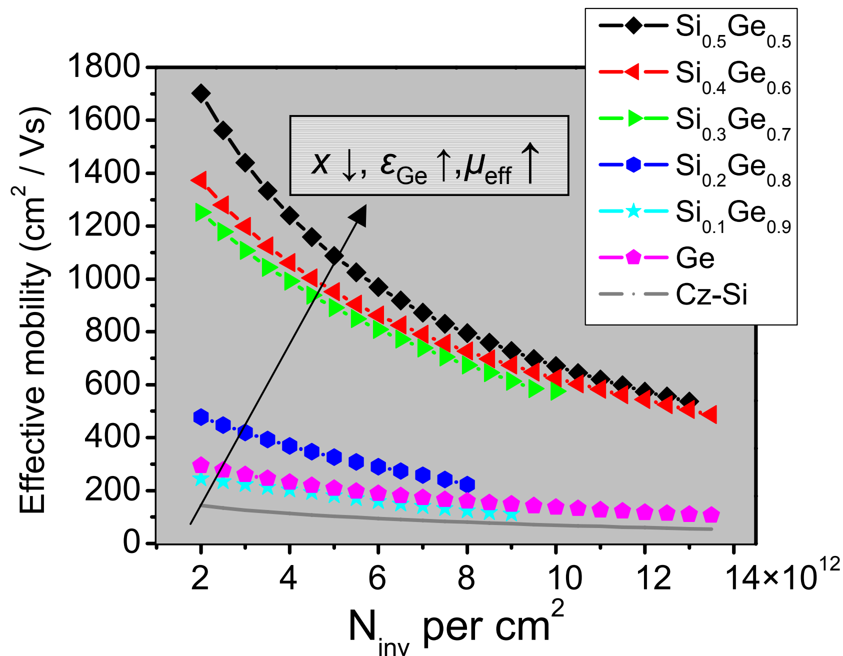


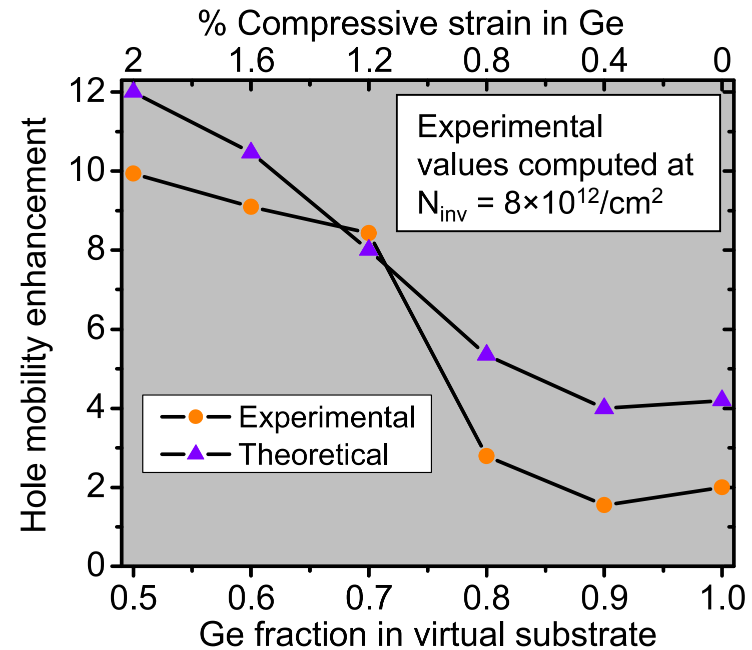




Donnelly, .., Banerjee, SRC 2004

Effect of strain in Ge layer



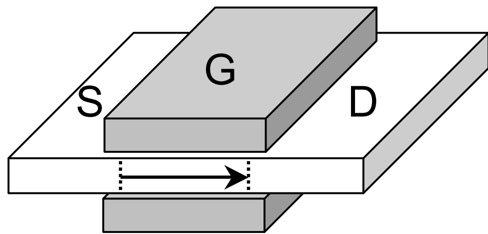


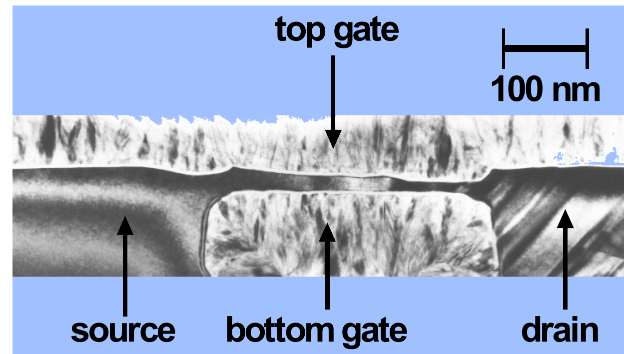
*Lee *et al.* *Appl. Phys. Lett*. **79**, 3344 (2001). Lee *et al.* in *Mater. Res. Soc. Symp*. Proc., vol. **686**, A1.9.1(2002).

- **Higher strain in the Ge layer favors high μ_{eff}***
  - $x \leq 0.7$
    - reasonable agreement with theoretical calculations**
  - $x \geq 0.8$
    - rampant defect nucleation in Si cap, μ_{eff} depressed

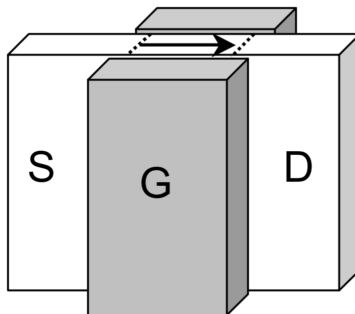
M. V. Fischetti and S. E. Laux, *J. Appl. Phys*. **80, (1996).

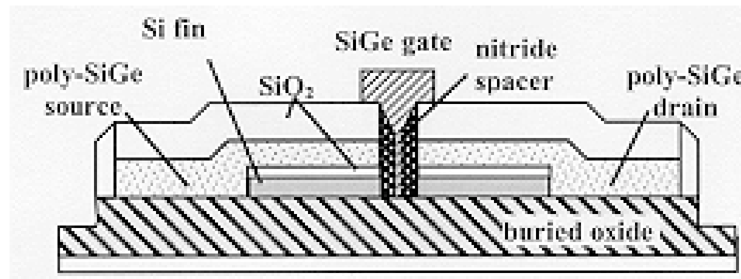
3-D Transistor Structures



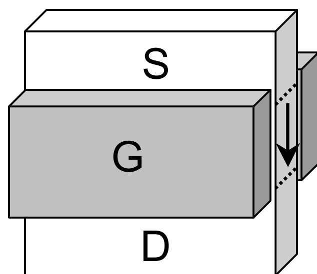


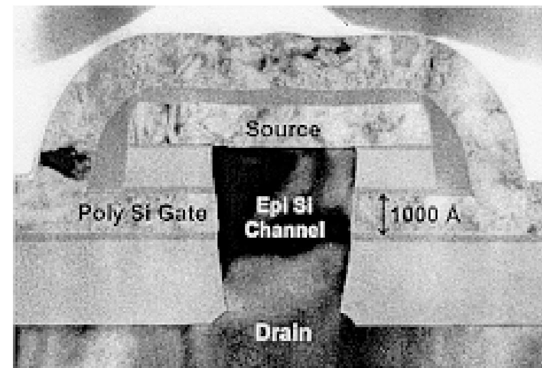
IBM ‘97





Berkeley ‘99

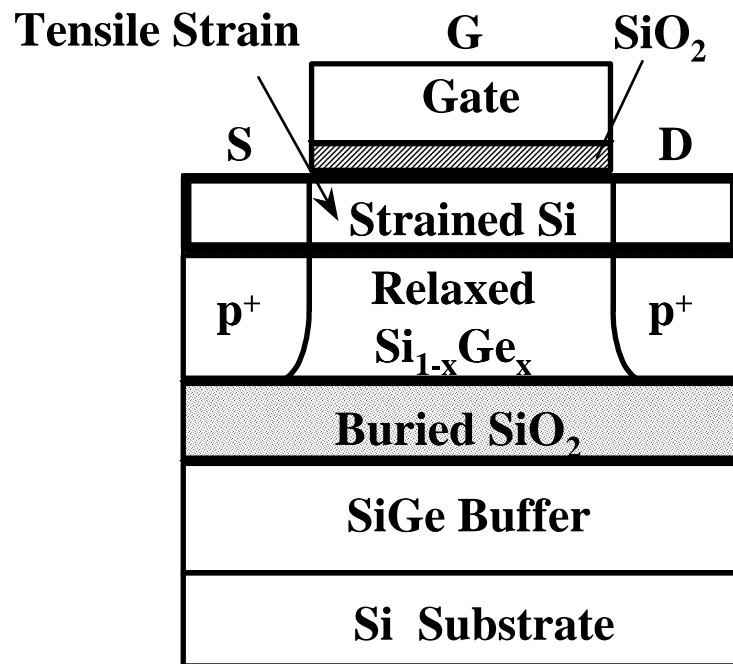


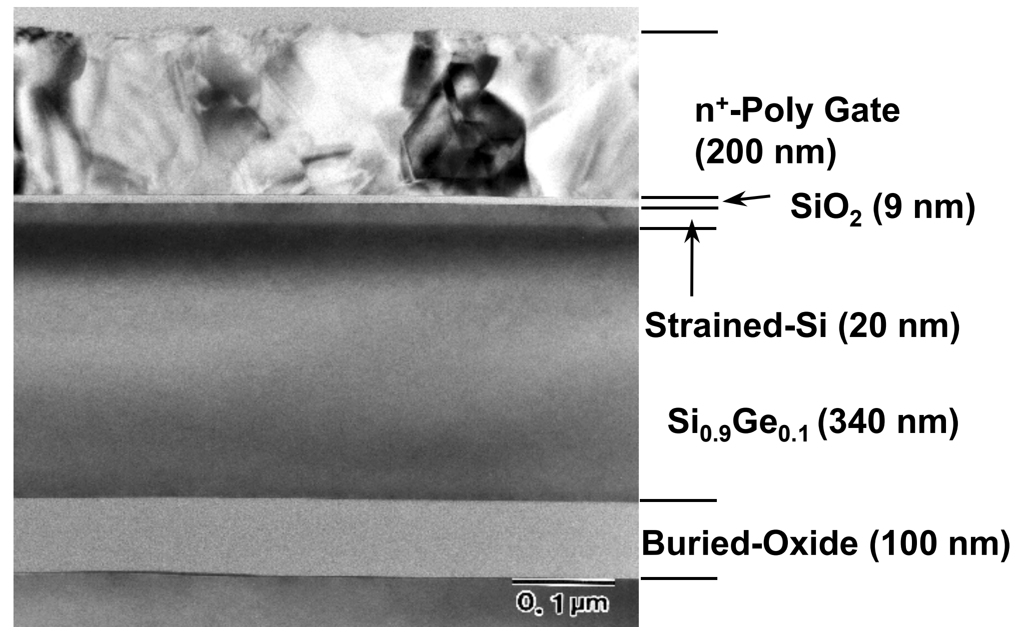


Lucent ‘99

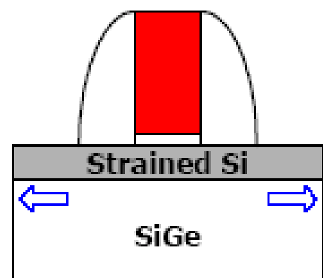
Mark Bohr, ECS Meeting PV 2001-2, Spring, 2001

Strained-Si PMOSFET on SiGe-on-Insulator

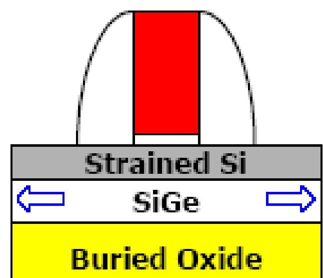




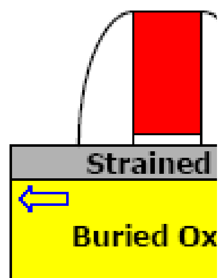
T. Mizuno et al., IEDM, 934-936 (1999)



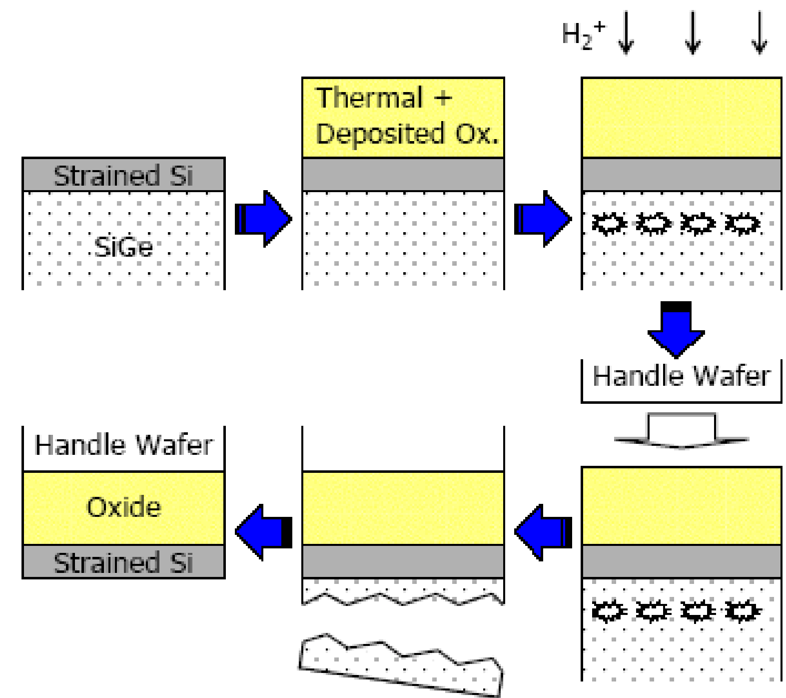
(a) Strained Si/SiGe Bulk MOSFET



(b) SGOI (SiGe-on-Insulator) MOSFET



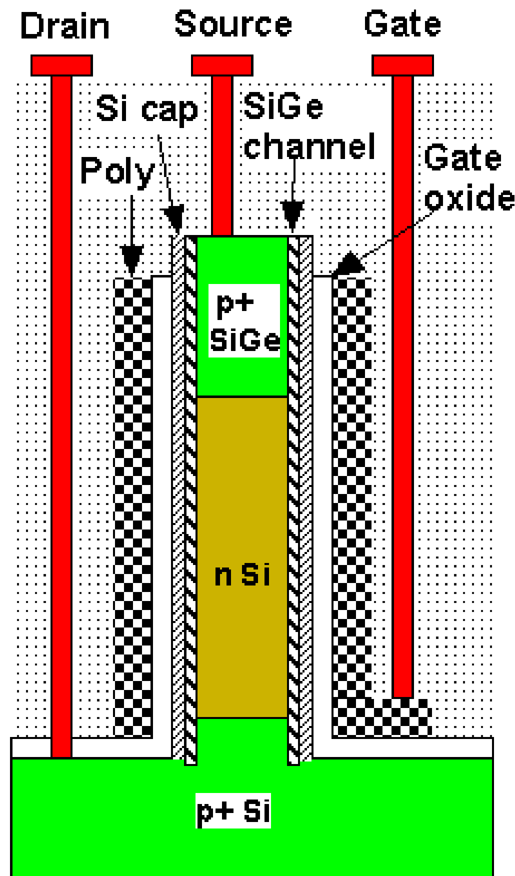
(c) **SSDOI** M



SSOI with thin SiGe buffers w/o misfits using BPSG compliant substrates

Rim, et. al. & Sturm et. al. (IEDM, 2003)

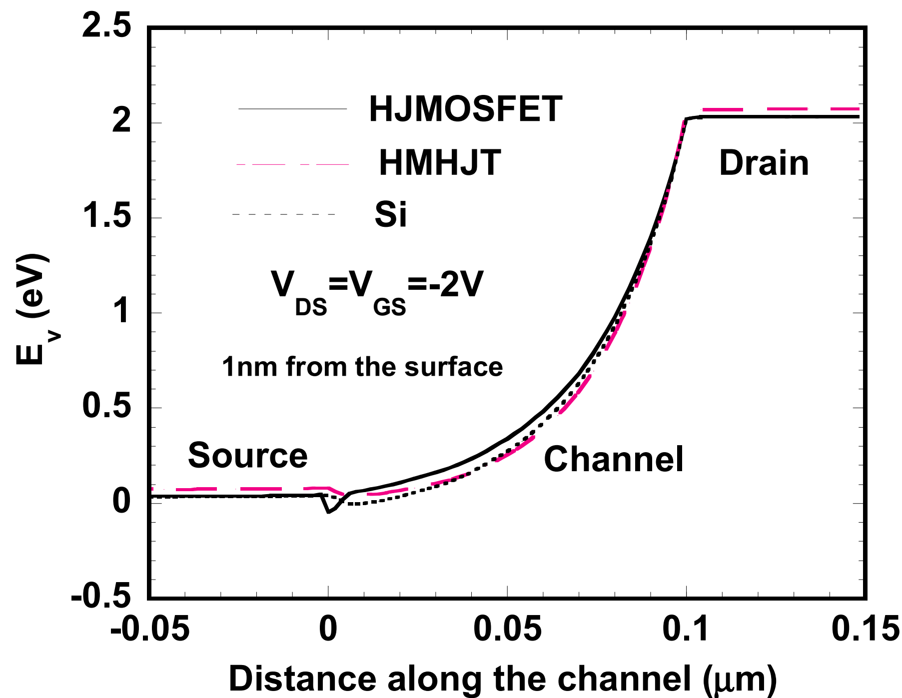
High mobility heterojunction transistor (HMHJT)

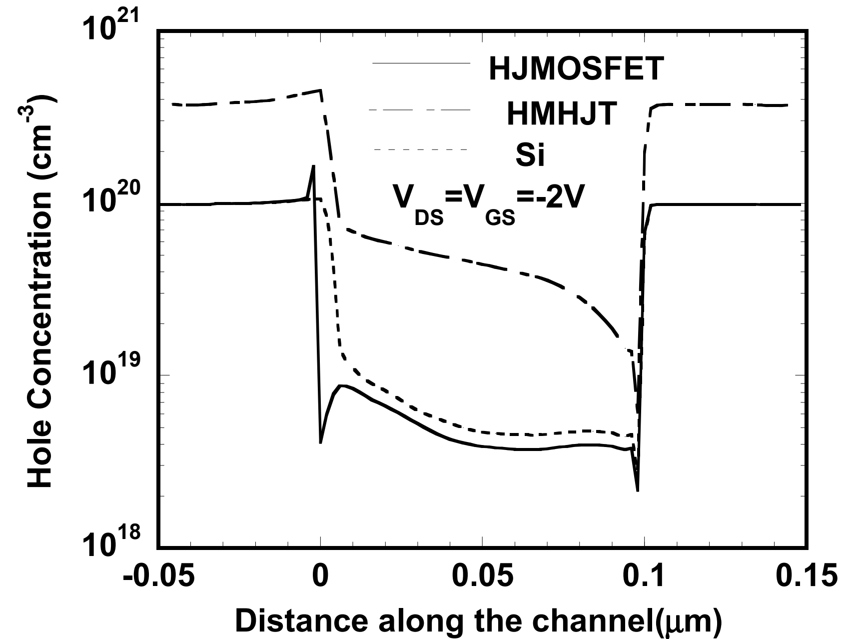


- **A Si/SiGe/Si quantum well is used to increase the drive current.**
- **The bulk punchthrough, DIBL and floating body effect are still suppressed due to heterojunction in the deep source/drain region.**

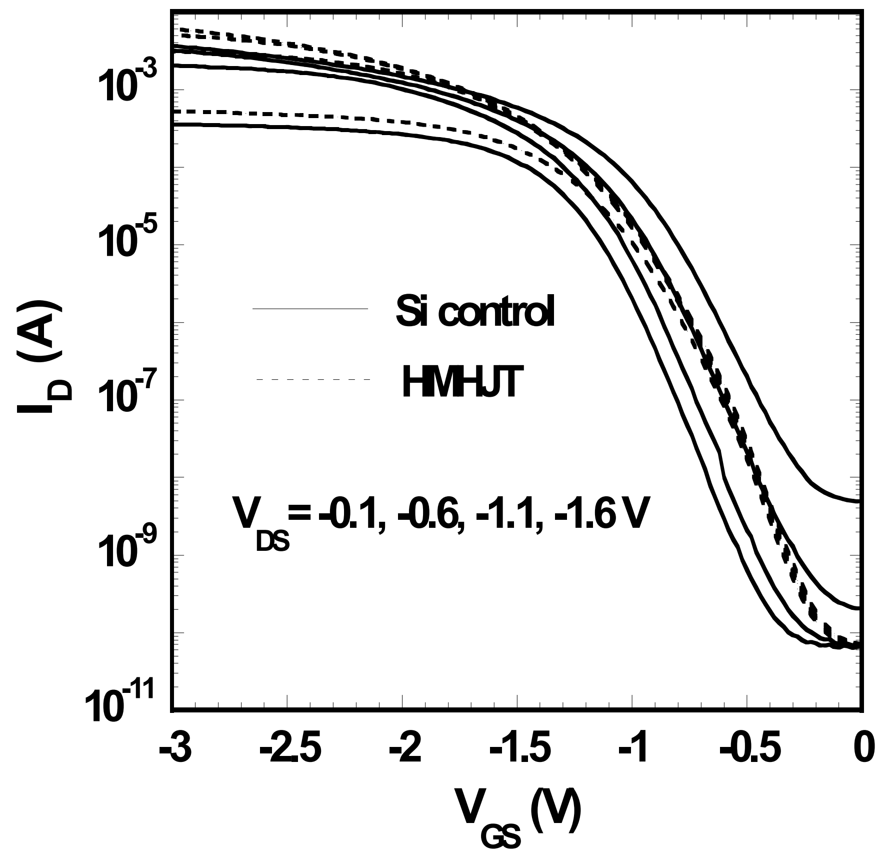
Q.Ouyang, X.Chen, ..A.Tasch, S.Banerjee, “Bandgap Engineering in Deep Submicron Vertical PMOSFETs,” Dev. Res. Conf., 2000.

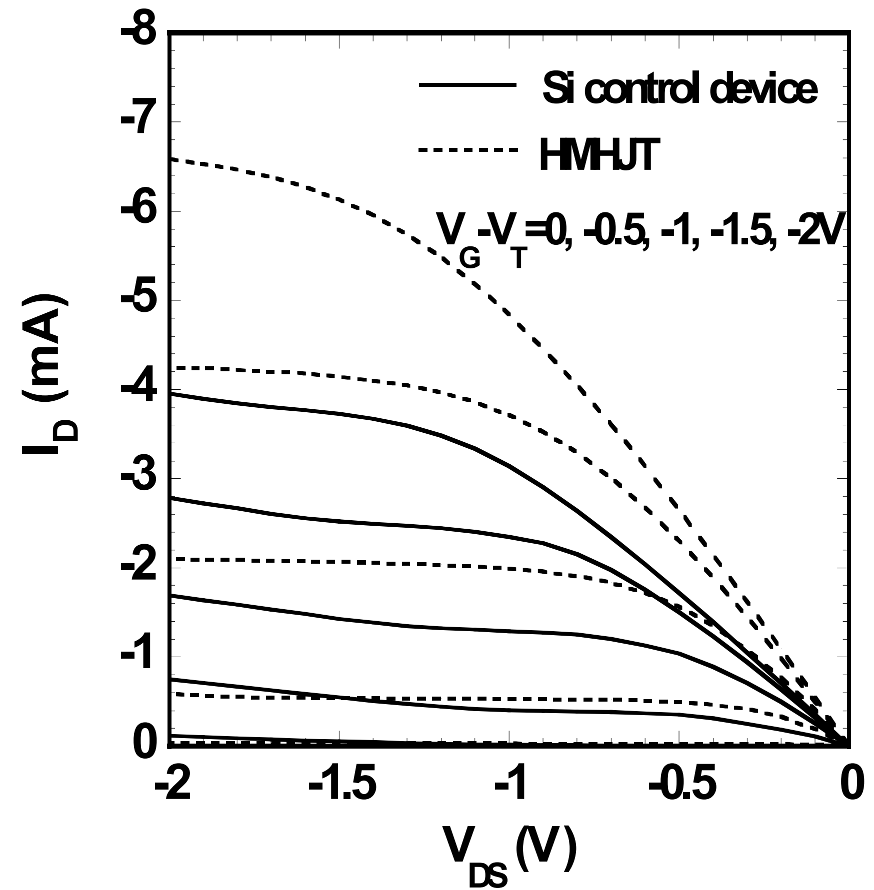
Energy Band Diagram and Hole Concentration of HMHJT in the Channel





Subthreshold and Output Characteristics for HMHJT



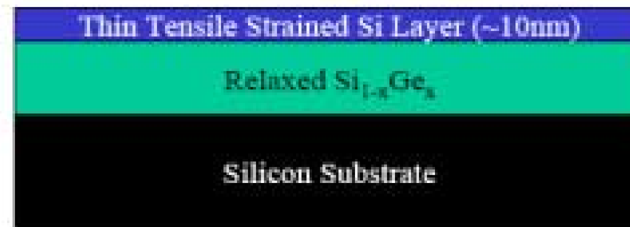


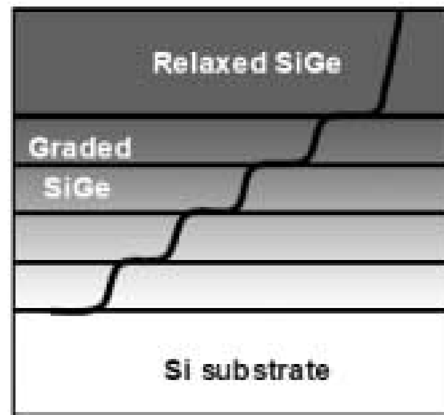
Process Issues

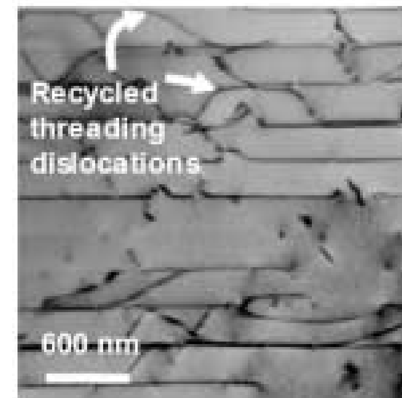
- Strain relaxation
  - Require low process temperature and thermal budget
- Leakage concerns
  - Defect/ dislocation density in active device layers
  - Smaller bandgap
- Self-heating
  - Much poorer thermal conductivity of SiGe layers
  - Thick gradual SiGe buffer layer

- STI edge leakage can be increased by SiGe buffer.
- B diffusion enhanced by tensile strain; compressive retards it.
  Ge retards B and enhances As/P diffusion in SiGe buffer.
- Need higher doping in channel due to reduced bandgap-
  negates some advantages of strain

Defects in Strained Si

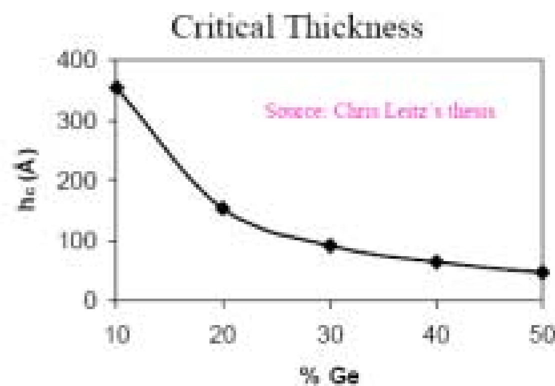


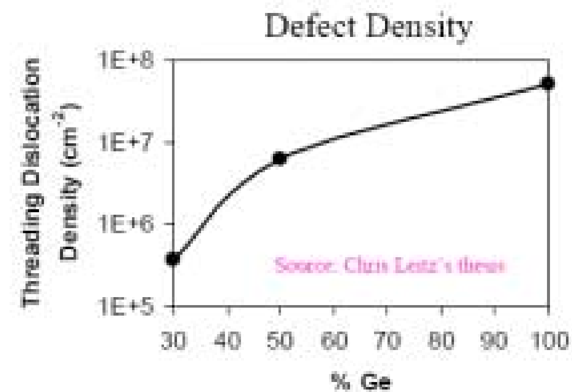




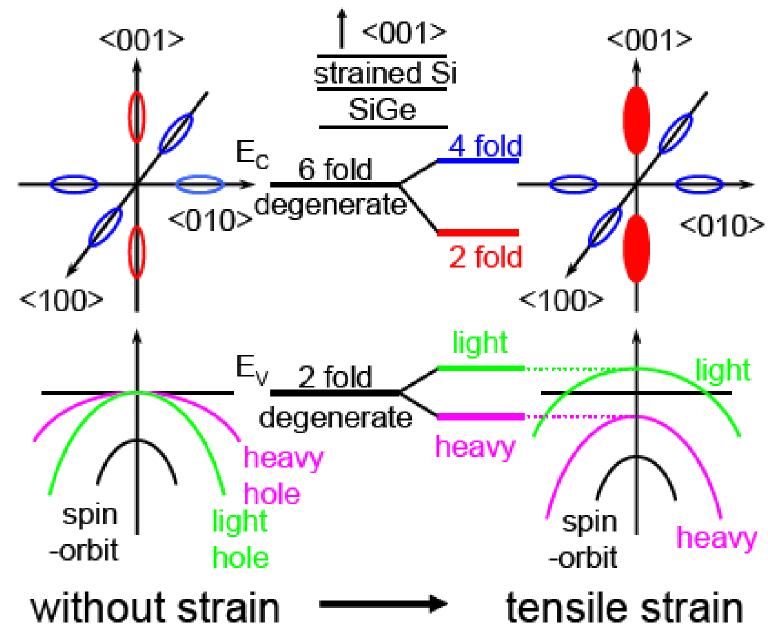
(a) Source: MIT/Fitzerald Group (b)

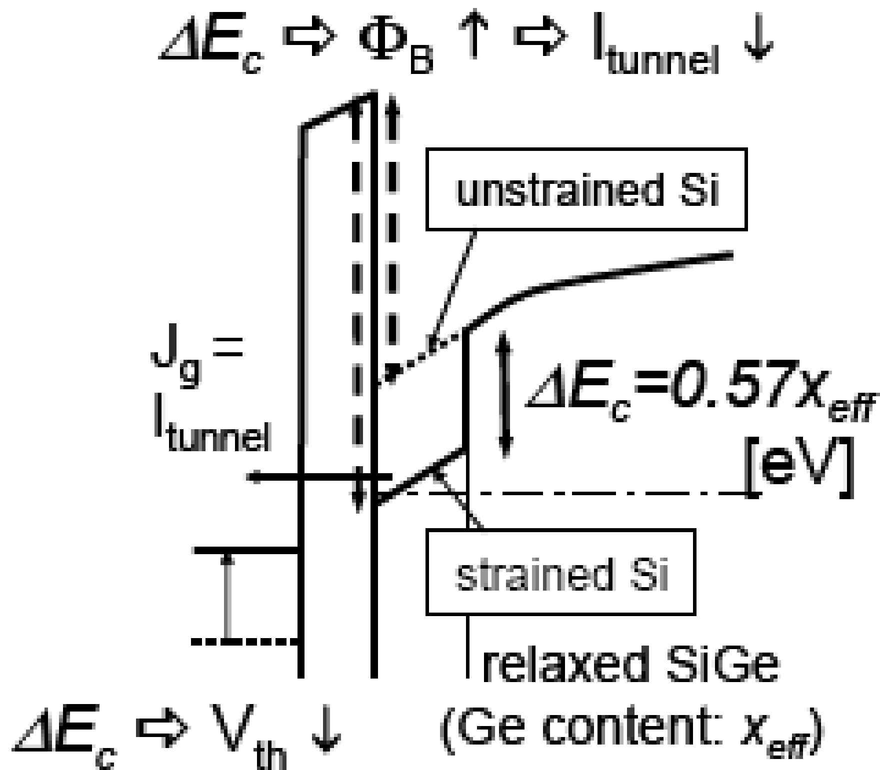
Strain: 1% mismatch ~ 1GPa, Si-Ge: 4%, Tensile in Si

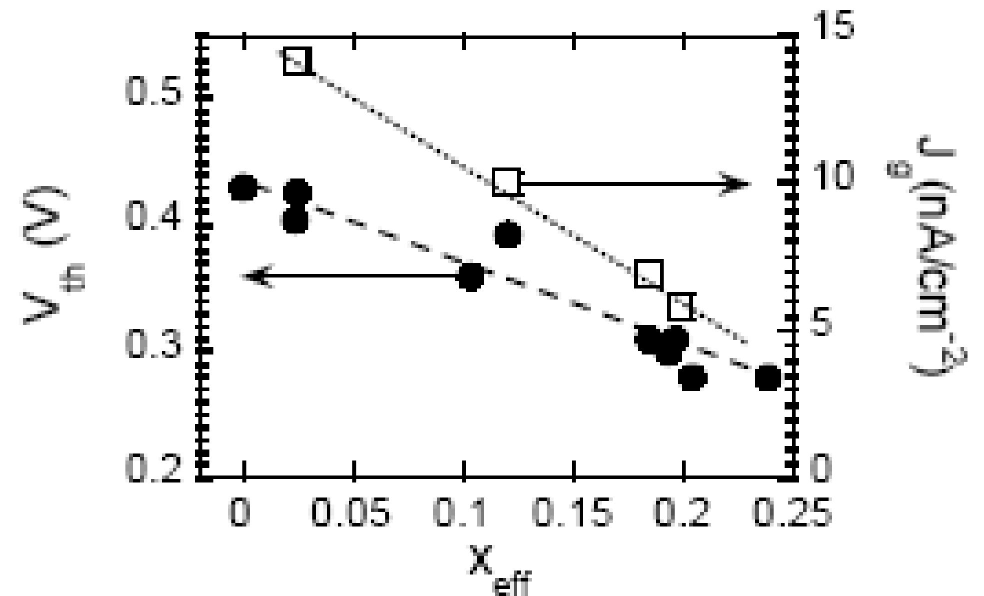




Takagi, et. al, IEDM 2003







Device Metrics

- Speed
  - $\tau = C_{load} V_{DD} / I_d$
- Power
  - $P = f C_{load} V_{DD}^2$
- Saturation current
  - $I_{DSAT} = (W/2L)(k_r k_o A)(T_{EOT,INV})^{-1} \mu (V_G - V_T)^2$
    - Consider $V_G \Rightarrow V_{DD}$
- Transconductance
  - $g_m = (W/L)(k_r k_o A)(T_{EOT,INV})^{-1} \mu V_{DSAT}$
- Off-state power
  - Subthreshold swing and source/drain junction leakage